

PAGE	CONTENTS
1	INDEX
2	BLOCK DIAGRAM
3	POWER DELIVERY
4	CHANGE LIST
5	CPU PCIEX16/DMI
6	CPU DDR CHANNEL A
7	CPU DDR CHANNEL B
8	CPU MISC
9	CPU POWER
10	CPU GND
11	DDR3 DIMMA1
12	DDR3 DIMMB1
13	PCH DMI/PCIE/USB
14	PCH CLINK/SATA/CPU HOST
15	PCH HDA/SPI/MISC
16	PCH LPC/DP/USB3/UART
17	PCH CLOCK BUFFER
18	PCH POWER
19	PCH GND
20	PCIEX16/X1*2 SLOT
21	RTD2168 EDP to VGA
22	DVI CONNECTOR
23	SIO IT8613E
24	SATA CONN
25	REAR USB
26	FRONT USB
27	LAN RTL8111H/8107E
28	AUDIO CODEC ALC887
29	AUDIO CONNECTOR
30	ACPI POWER
31	MEMORY DC-DC
32	V_1P0_PCH
33	RESUME RESET LOGIC
34	SUPERIO PS2/COM
35	FAN
36	24PIN CONN & FP
37	SPI ROM/RTC CRYSTAL/BAT
38	VCCIO/VCCSA DC-DC
39	RT3606 DC-DC CONVERTE
40	RT3606_VCORE_PHASE
41	RT3606_VGT_PHASE
42	BOM

IH11P-MHS H110MDS2 PRO D4 VER 6.0

CPU:

Intel Skylake S 42 in LGA1151 Package 95W

System Chipset:

SPT-H PCH

Main Memory:

Dual Channel/DDR-4*2(Max 16GB)1867/2133

Onboard Device:

Super I/O:IT8613E

LAN:Realtek 8111H

HD Codec:ALC887

Power solution:

CPU Voltage Regulators:3phase by RT3606

DDR Voltage Regulators:1Phase by UP1514

high 1 Low 1 OV by RT3606

high 1 Low 1 OV by IT8613E

Expansion Slots:

PCI EXPRESS 16X SLOT *1

PCI EXPRESS 1X SLOT *2

REAR IO:

PS/2 PORT

DVI Port

VGA Port

USB3.0 PORT *2

Gb RJ-45 +2 layer USB3.0 Ports

Audio Jackets (3 PORT)

Front I/O:

SATA3 *6

USB 2.0 Header * 2

Serial header

USB 3.0 Header * 1

Front Audio Header

CPU FAN *1

System FAN *1

◇BIOSTAR'S PROPRIETARY
INFORMATION◇

◇Any unauthorized use, reproduction,
duplication, or disclosure of this document
will be subject to the applicable civil
and/criminal penalties.◇



映泰股份有限公司
BIOSSTAR GROUP

Title			INDEX
Size	Document Number	IH11P-MHS	
B			Rev 6.0
Date:	Friday, January 15, 2016	Sheet 1	of 42

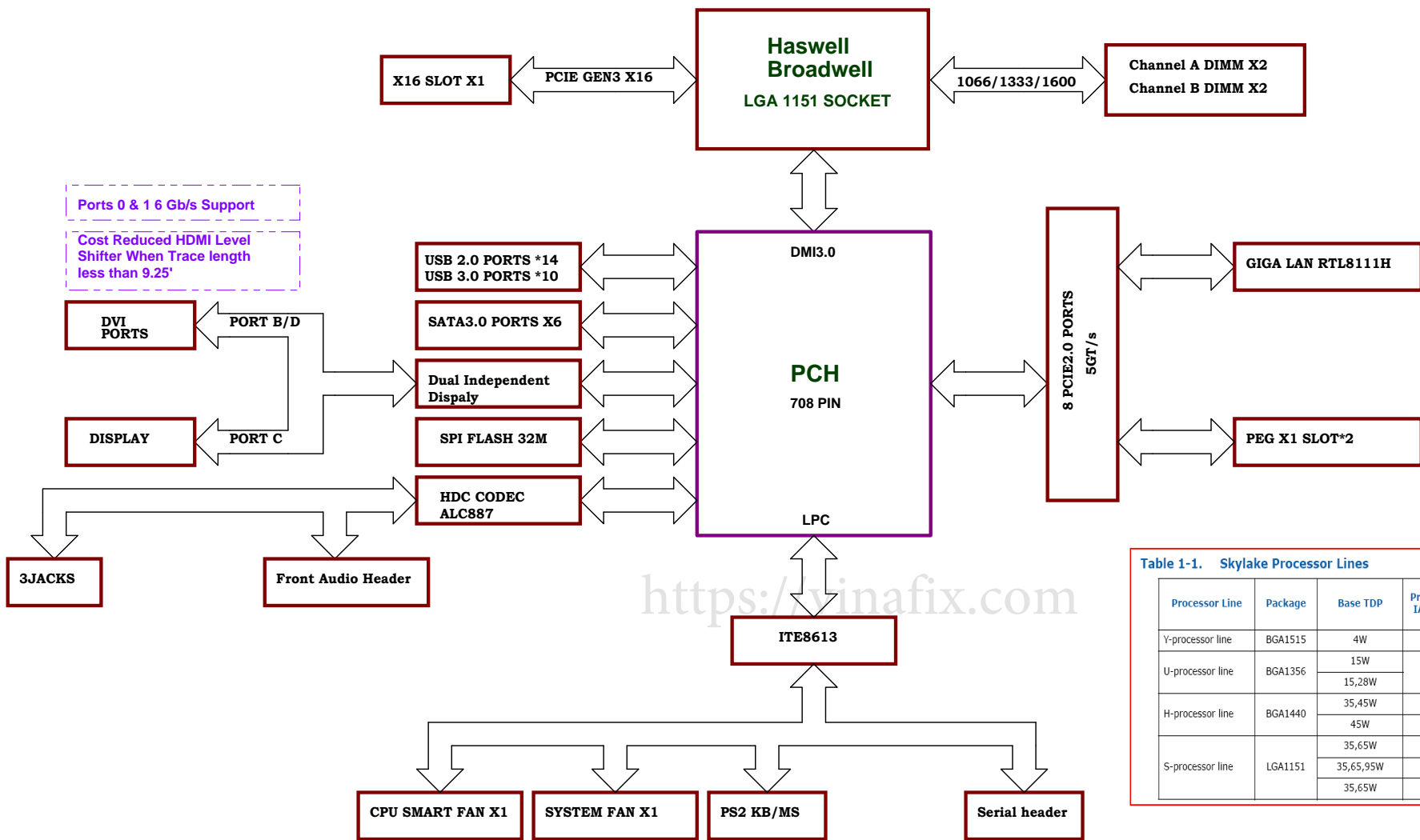
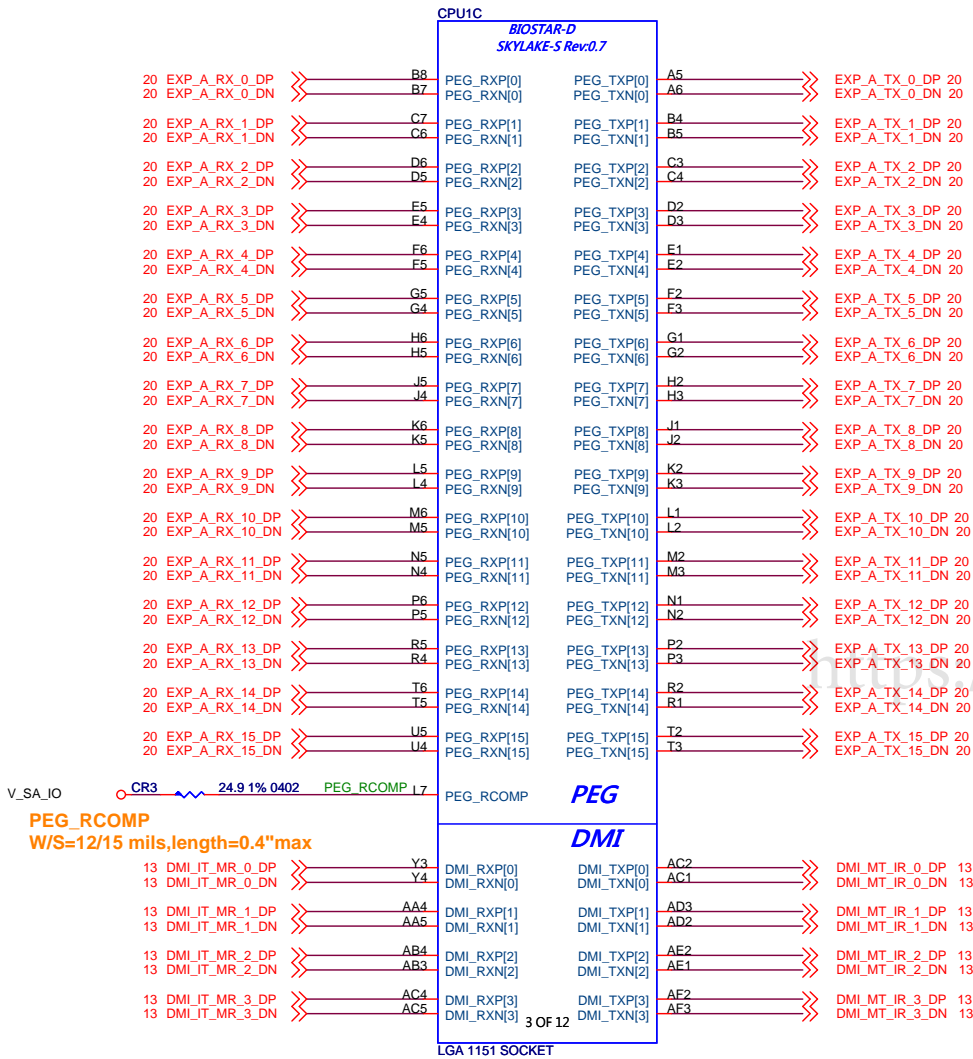
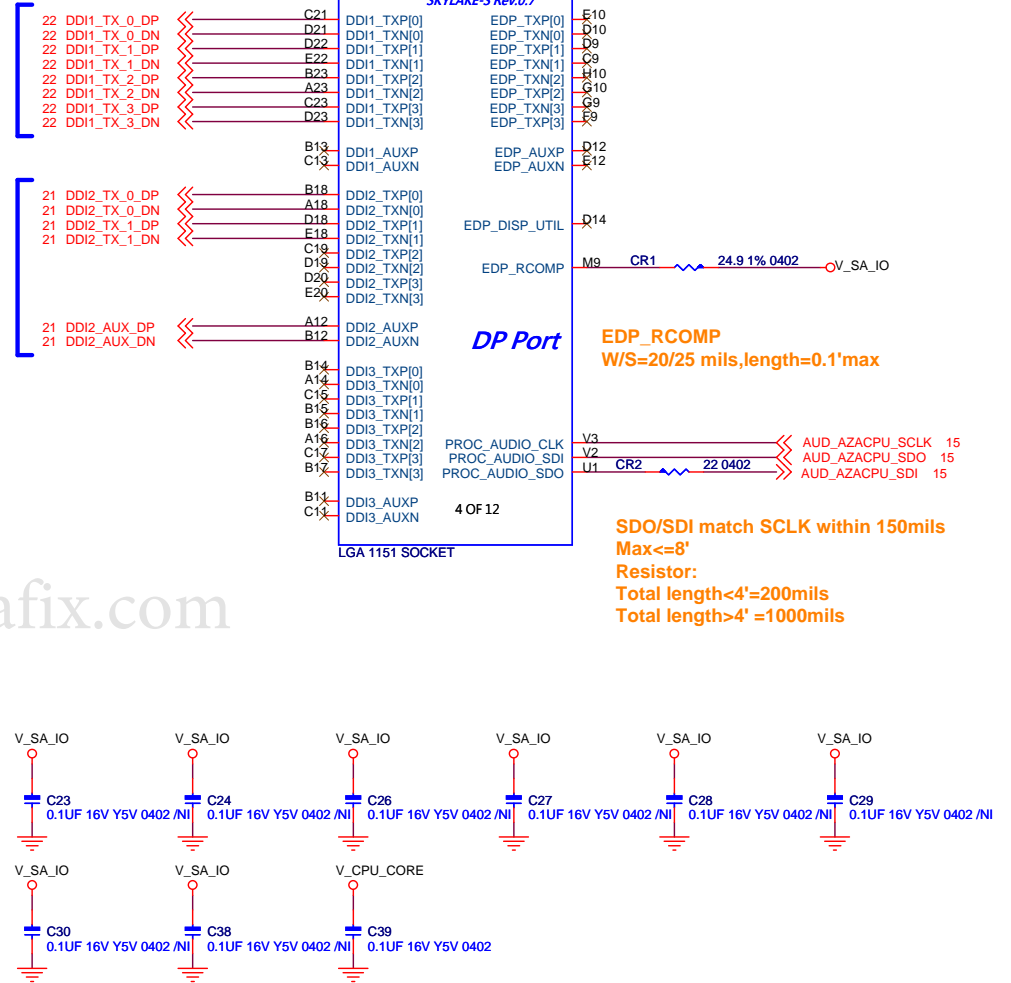


Table 1-1. Skylake Processor Lines						
Processor Line	Package	Base TDP	Processor IA Cores	Maximum Graphics Configuration	On Package Cache	Platform Type
Y-processor line	BGA1515	4W	2	GT2	N/A	1-Chip
U-processor line	BGA1356	15W	2	GT2	64 MB	1-Chip
		15,28W		GT3		
H-processor line	BGA1440	35,45W	4	GT2	N/A	2-Chip
		45W	4	GT4	128 MB	
S-processor line	LGA1151	35,65W	2	GT2	N/A	2-Chip
		35,65,95W	4	GT2		
		35,65W	4	GT4	64 MB	



DVI PORT

EDP to VGA



◇BIOSTAR'S PROPRIETARY INFORMATION◇

◇Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties.◇



映泰股份有限公司
BIOSTAR GROUP

Title			
CPU PCIEX16/DMI/FDI			
Size	Document Number		Rev
B	IH11P-MHS		6.0
Date: Friday, January 15, 2016		Sheet	5 of 42

12 M_DATA_B[0..63] <<< M_DATA_B[0..63]

M_DATA_B0 AD34
M_DATA_B1 AD35
M_DATA_B2 AG35
M_DATA_B3 AH35
M_DATA_B4 AE35
M_DATA_B5 AE34
M_DATA_B6 AG34
M_DATA_B7 AH34
M_DATA_B8 AK35
M_DATA_B9 AL35
M_DATA_B10 AK32
M_DATA_B11 AL32
M_DATA_B12 AK34
M_DATA_B13 AL34
M_DATA_B14 AK31
M_DATA_B15 AL31
M_DATA_B16 AP35
M_DATA_B17 AN35
M_DATA_B18 AN32
M_DATA_B19 AP32
M_DATA_B20 AN34
M_DATA_B21 AP34
M_DATA_B22 AN31
M_DATA_B23 AP31
M_DATA_B24 AL28
M_DATA_B25 AM28
M_DATA_B26 AR28
M_DATA_B27 AR29
M_DATA_B28 AM28
M_DATA_B29 AL28
M_DATA_B30 AR28
M_DATA_B31 AP28
M_DATA_B32 AR12
M_DATA_B33 AP12
M_DATA_B34 AM13
M_DATA_B35 AL13
M_DATA_B36 AR13
M_DATA_B37 AP13
M_DATA_B38 AM12
M_DATA_B39 AL12
M_DATA_B40 AP10
M_DATA_B41 AR10
M_DATA_B42 AR7
M_DATA_B43 AP7
M_DATA_B44 AR9
M_DATA_B45 AP9
M_DATA_B46 AR6
M_DATA_B47 AP6
M_DATA_B48 AM10
M_DATA_B49 AL10
M_DATA_B50 AM7
M_DATA_B51 AL7
M_DATA_B52 AM9
M_DATA_B53 AL9
M_DATA_B54 AM6
M_DATA_B55 AL6
M_DATA_B56 AJ6
M_DATA_B57 AJ7
M_DATA_B58 AE6
M_DATA_B59 AE7
M_DATA_B60 AH7
M_DATA_B61 AH6
M_DATA_B62 AE7
M_DATA_B63 AF6

AR25 DDR1_ECC[0]
AR26 DDR1_ECC[1]
AM26 DDR1_ECC[2]
AM25 DDR1_ECC[3]
AP26 DDR1_ECC[4]
AP25 DDR1_ECC[5]
AL25 DDR1_ECC[6]
AL26 DDR1_ECC[7]

CPU1B

BIOSTAR-D
SKYLAKE-5
Rev:0.7

DDR CHANNEL B

DDR1_DQ[0]/DDR0_DQ[16]
DDR1_DQ[1]/DDR0_DQ[17]
DDR1_DQ[2]/DDR0_DQ[18]
DDR1_DQ[3]/DDR0_DQ[19]
DDR1_DQ[4]/DDR0_DQ[20]
DDR1_DQ[5]/DDR0_DQ[21]
DDR1_DQ[6]/DDR0_DQ[22]
DDR1_DQ[7]/DDR0_DQ[23]
DDR1_DQ[8]/DDR0_DQ[24]
DDR1_DQ[9]/DDR0_DQ[25]
DDR1_DQ[10]/DDR0_DQ[26]
DDR1_DQ[11]/DDR0_DQ[27]
DDR1_DQ[12]/DDR0_DQ[28]
DDR1_DQ[13]/DDR0_DQ[29]
DDR1_DQ[14]/DDR0_DQ[30]
DDR1_DQ[15]/DDR0_DQ[31]
DDR1_DQ[16]/DDR0_DQ[48]
DDR1_DQ[17]/DDR0_DQ[49]
DDR1_DQ[18]/DDR0_DQ[50]
DDR1_DQ[19]/DDR0_DQ[51]
DDR1_DQ[20]/DDR0_DQ[52]
DDR1_DQ[21]/DDR0_DQ[53]
DDR1_DQ[22]/DDR0_DQ[54]
DDR1_DQ[23]/DDR0_DQ[55]
DDR1_DQ[24]/DDR0_DQ[56]
DDR1_DQ[25]/DDR0_DQ[57]
DDR1_DQ[26]/DDR0_DQ[58]
DDR1_DQ[27]/DDR0_DQ[59]
DDR1_DQ[28]/DDR0_DQ[60]
DDR1_DQ[29]/DDR0_DQ[61]
DDR1_DQ[30]/DDR0_DQ[62]
DDR1_DQ[31]/DDR0_DQ[63]
DDR1_DQ[32]/DDR1_DQ[16]
DDR1_DQ[33]/DDR1_DQ[17]
DDR1_DQ[34]/DDR1_DQ[18]
DDR1_DQ[35]/DDR1_DQ[19]
DDR1_DQ[36]/DDR1_DQ[20]
DDR1_DQ[37]/DDR1_DQ[21]
DDR1_DQ[38]/DDR1_DQ[22]
DDR1_DQ[39]/DDR1_DQ[23]
DDR1_DQ[40]/DDR1_DQ[24]
DDR1_DQ[41]/DDR1_DQ[25]
DDR1_DQ[42]/DDR1_DQ[26]
DDR1_DQ[43]/DDR1_DQ[27]
DDR1_DQ[44]/DDR1_DQ[28]
DDR1_DQ[45]/DDR1_DQ[29]
DDR1_DQ[46]/DDR1_DQ[30]
DDR1_DQ[47]/DDR1_DQ[31]
DDR1_DQ[48]
DDR1_DQ[49]
DDR1_DQ[50]
DDR1_DQ[51]
DDR1_DQ[52]
DDR1_DQ[53]
DDR1_DQ[54]
DDR1_DQ[55]
DDR1_DQ[56]
DDR1_DQ[57]
DDR1_DQ[58]
DDR1_DQ[59]
DDR1_DQ[60]
DDR1_DQ[61]
DDR1_DQ[62]
DDR1_DQ[63]
DDR1_ECC[0]
DDR1_ECC[1]
DDR1_ECC[2]
DDR1_ECC[3]
DDR1_ECC[4]
DDR1_ECC[5]
DDR1_ECC[6]
DDR1_ECC[7]

2 OF 12

LGA 1151 SOCKET

DDR1_CKP[0]
DDR1_CKN[0]
DDR1_CKP[1]
DDR1_CKN[1]
DDR1_CKP[2]
DDR1_CKN[2]
DDR1_CKP[3]
DDR1_CKN[3]

DDR1_CKE[0]
DDR1_CKE[1]
DDR1_CKE[2]
DDR1_CKE[3]

DDR1_CS#[0]
DDR1_CS#[1]
DDR1_CS#[2]
DDR1_CS#[3]

DDR1_ODT[0]
DDR1_ODT[1]
DDR1_ODT[2]
DDR1_ODT[3]

DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]

DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]
DDR1_BA[2]/DDR1_CAB[5]/DDR1_BG[0]

DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]
DDR1_MA[3]
DDR1_MA[4]

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]
DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#

DDR1_PAR
DDR1_ALERT#

DDR1_DQSN[0]/DDR0_DQSN[2]
DDR1_DQSN[1]/DDR0_DQSN[3]
DDR1_DQSN[2]/DDR0_DQSN[6]
DDR1_DQSN[3]/DDR0_DQSN[7]
DDR1_DQSN[4]/DDR1_DQSN[2]
DDR1_DQSN[5]/DDR1_DQSN[3]
DDR1_DQSN[6]
DDR1_DQSN[7]

DDR1_DQSP[0]/DDR0_DQSP[2]
DDR1_DQSP[1]/DDR0_DQSP[3]
DDR1_DQSP[2]/DDR0_DQSP[6]
DDR1_DQSP[3]/DDR0_DQSP[7]
DDR1_DQSP[4]/DDR1_DQSP[2]
DDR1_DQSP[5]/DDR1_DQSP[3]
DDR1_DQSP[6]
DDR1_DQSP[7]

DDR1_DQSP[8]
DDR1_DQSN[8]

DDR_VREF_CA
DDR0_VREF_DQ
DDR1_VREF_DQ

AM20 >>> CK_M_CH1_0_DP 12
AM21 >>> CK_M_CH1_0_DN 12
AP22 >>> CK_M_CH1_1_DP 12
AP21 >>> CK_M_CH1_1_DN 12
AN20
AN21
AP19
AP20

AY29 >>> M_SCKE_B0 12
AV29 >>> M_SCKE_B1 12
AW29
AU29

AP17 >>> M_SCS_B_N0 12
AN15 >>> M_SCS_B_N1 12
AN17
AM15

AL16 >>> M_ODT_B0 12
AL16 >>> M_ODT_B1 12
AP15
AL15

AN18 M_MAA_B16 >>> M_MAA_B[0..16] 12
AL17 M_MAA_B14 >>> M_MAA_B[0..16] 12
AP16 M_MAA_B15 >>> M_MAA_B[0..16] 12

AL18 >>> M_SBS_B0 12
AM18 >>> M_SBS_B1 12
AW28 >>> M_BG_CH1_0 12

AL19 M_MAA_B0 >>> M_MAA_B[0..16] 12
AL22 M_MAA_B1 >>> M_MAA_B[0..16] 12
AM22 M_MAA_B2 >>> M_MAA_B[0..16] 12
AM23 M_MAA_B3 >>> M_MAA_B[0..16] 12
AP23 M_MAA_B4 >>> M_MAA_B[0..16] 12
AL23 M_MAA_B5 >>> M_MAA_B[0..16] 12
AW26 M_MAA_B6 >>> M_MAA_B[0..16] 12
AY26 M_MAA_B7 >>> M_MAA_B[0..16] 12
AU26 M_MAA_B8 >>> M_MAA_B[0..16] 12
AW27 M_MAA_B9 >>> M_MAA_B[0..16] 12
AP18 M_MAA_B10 >>> M_MAA_B[0..16] 12
AU27 M_MAA_B11 >>> M_MAA_B[0..16] 12
AV27 M_MAA_B12 >>> M_MAA_B[0..16] 12
AR15 M_MAA_B13 >>> M_MAA_B[0..16] 12
AY28 >>> M_BG_CH1_1 12
AU28 >>> DDR_CH1_ACT_N 12

AL20 >>> DDR_CH1_PAR 12
AY25 >>> DDR_CH1_ALERT_N 12

AF34 >>> M_DQS_B_DN0 12
AK33 >>> M_DQS_B_DN1 12
AN33 >>> M_DQS_B_DN2 12
AN29 >>> M_DQS_B_DN3 12
AN13 >>> M_DQS_B_DN4 12
AR8 >>> M_DQS_B_DN5 12
AM8 >>> M_DQS_B_DN6 12
AG6 >>> M_DQS_B_DN7 12

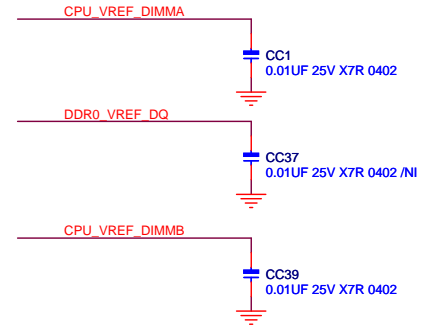
AF35 >>> M_DQS_B_DP0 12
AL33 >>> M_DQS_B_DP1 12
AP33 >>> M_DQS_B_DP2 12
AN28 >>> M_DQS_B_DP3 12
AN12 >>> M_DQS_B_DP4 12
AP8 >>> M_DQS_B_DP5 12
AL8 >>> M_DQS_B_DP6 12
AG7 >>> M_DQS_B_DP7 12


AB40 CPU_VREF_DIMMA <<< CPU_VREF_DIMMA 11
AC40 DDR0_VREF_DQ <<< CPU_VREF_DIMMA 11
AC39 CPU_VREF_DIMMB <<< CPU_VREF_DIMMB 12

M_DQS_B_DP[0..7] <<< M_DQS_B_DP[0..7] 12

M_DQS_B_DN[0..7] <<< M_DQS_B_DN[0..7] 12

VER0.60:DDR3 CHANGE DDR4(PAGE6/7/11/12)





映泰股份有限公司

BIOS STAR GROUP

Title

CPU DDR3 CHANNEL B

Size B

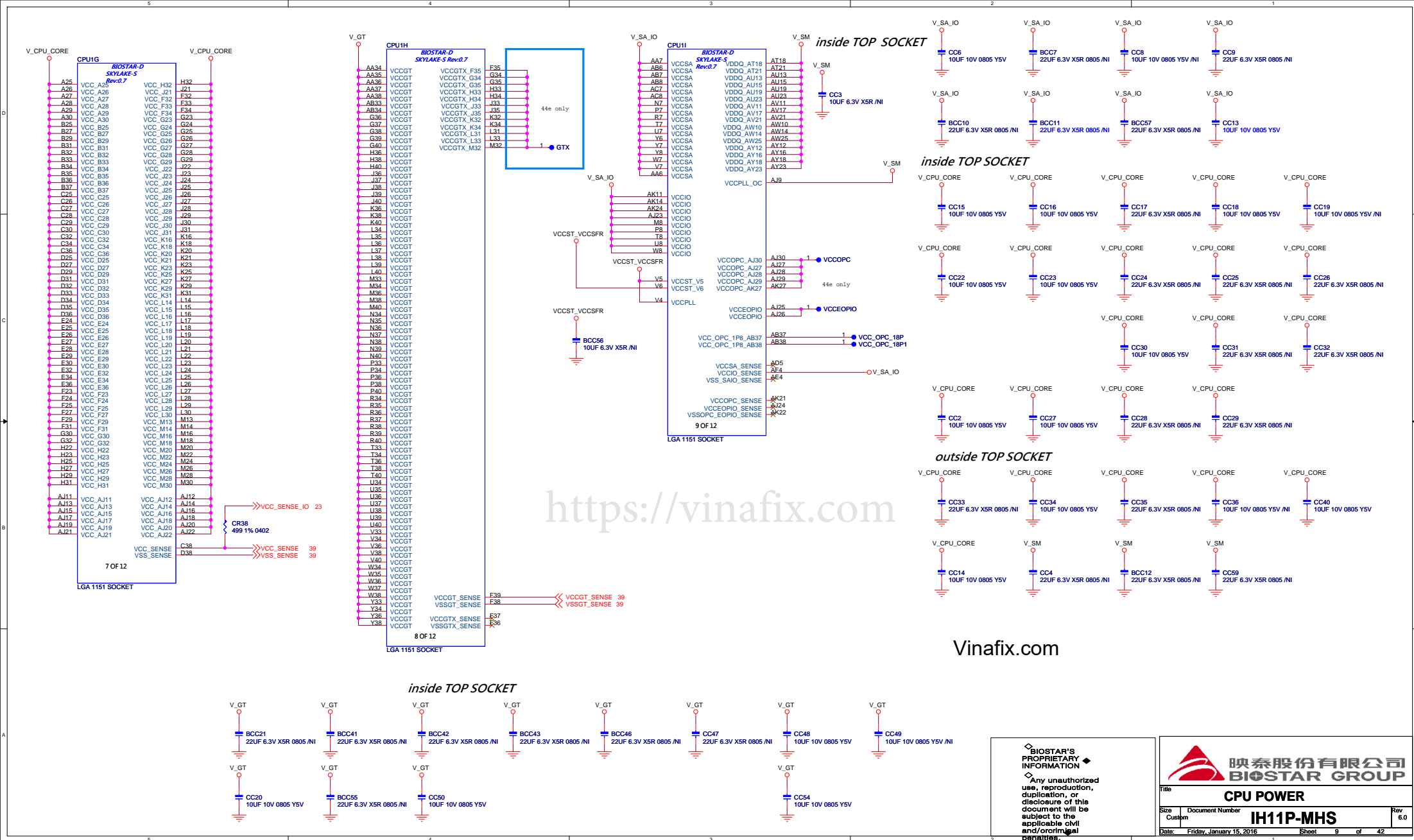
Document Number

IH11P-MHS

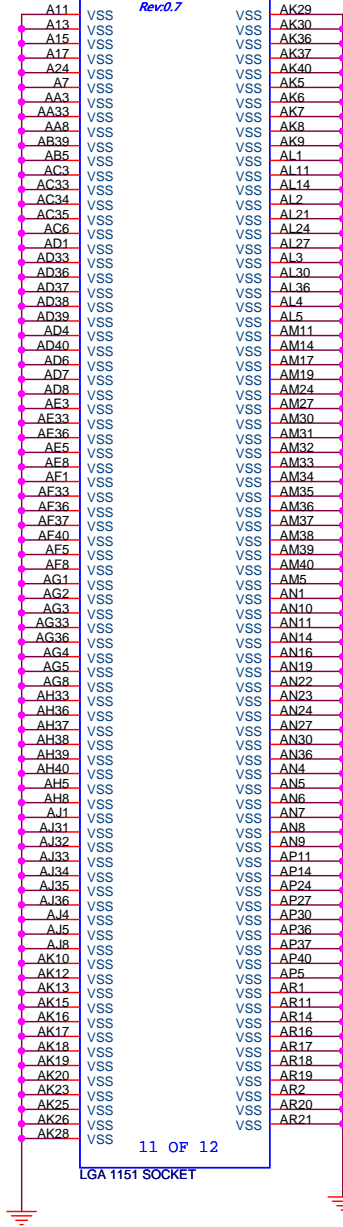
Rev 6.0

Date: Friday, January 15, 2016

Sheet 7 of 42



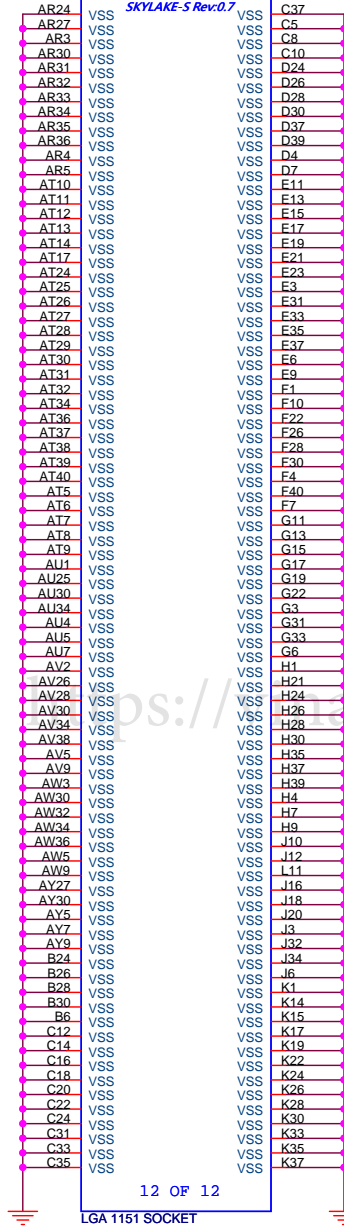
CPU1K

BIOSTAR-D
SKYLAKE-S
Rev.0.7

11 OF 12

LGA 1151 SOCKET

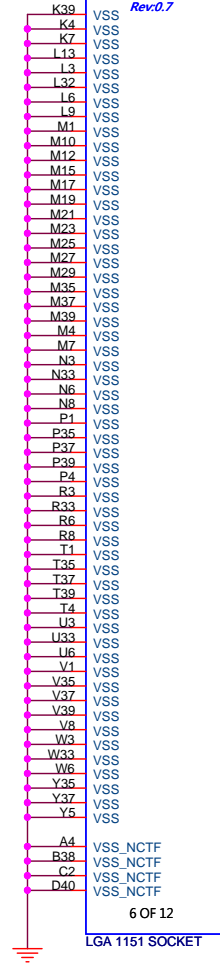
CPU1L

BIOSTAR-D
SKYLAKE-S Rev.0.7

12 OF 12

LGA 1151 SOCKET

CPU1F

BIOSTAR-D
SKYLAKE-S
Rev.0.7

6 OF 12

LGA 1151 SOCKET

◆BIOSTAR'S PROPRIETARY
INFORMATION◆◆Any unauthorized use,
reproduction, duplication, or
disclosure of this document
will be subject to the
applicable civil and/or criminal
penalties.◆映泰股份有限公司
BIOSTAR GROUP

Title

CPU GND

Size
B

Document Number

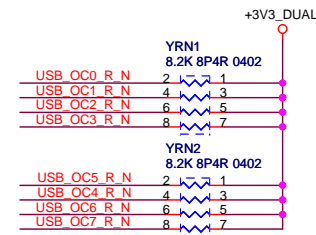
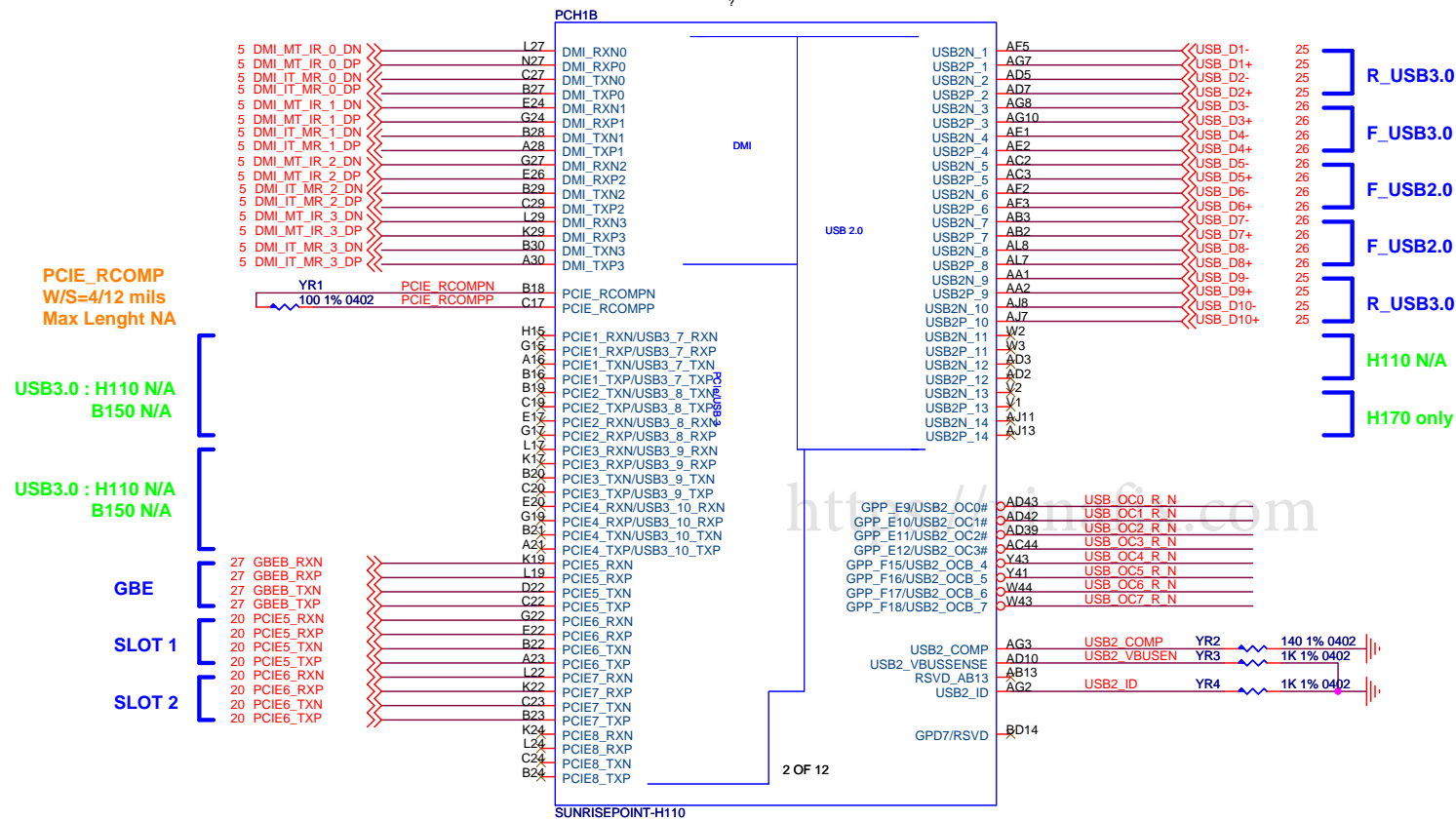
IH11P-MHS

Rev
6.0

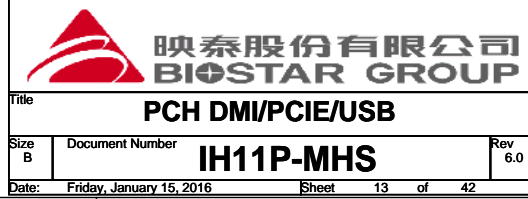
Date: Friday, January 15, 2016

Sheet 10 of 42

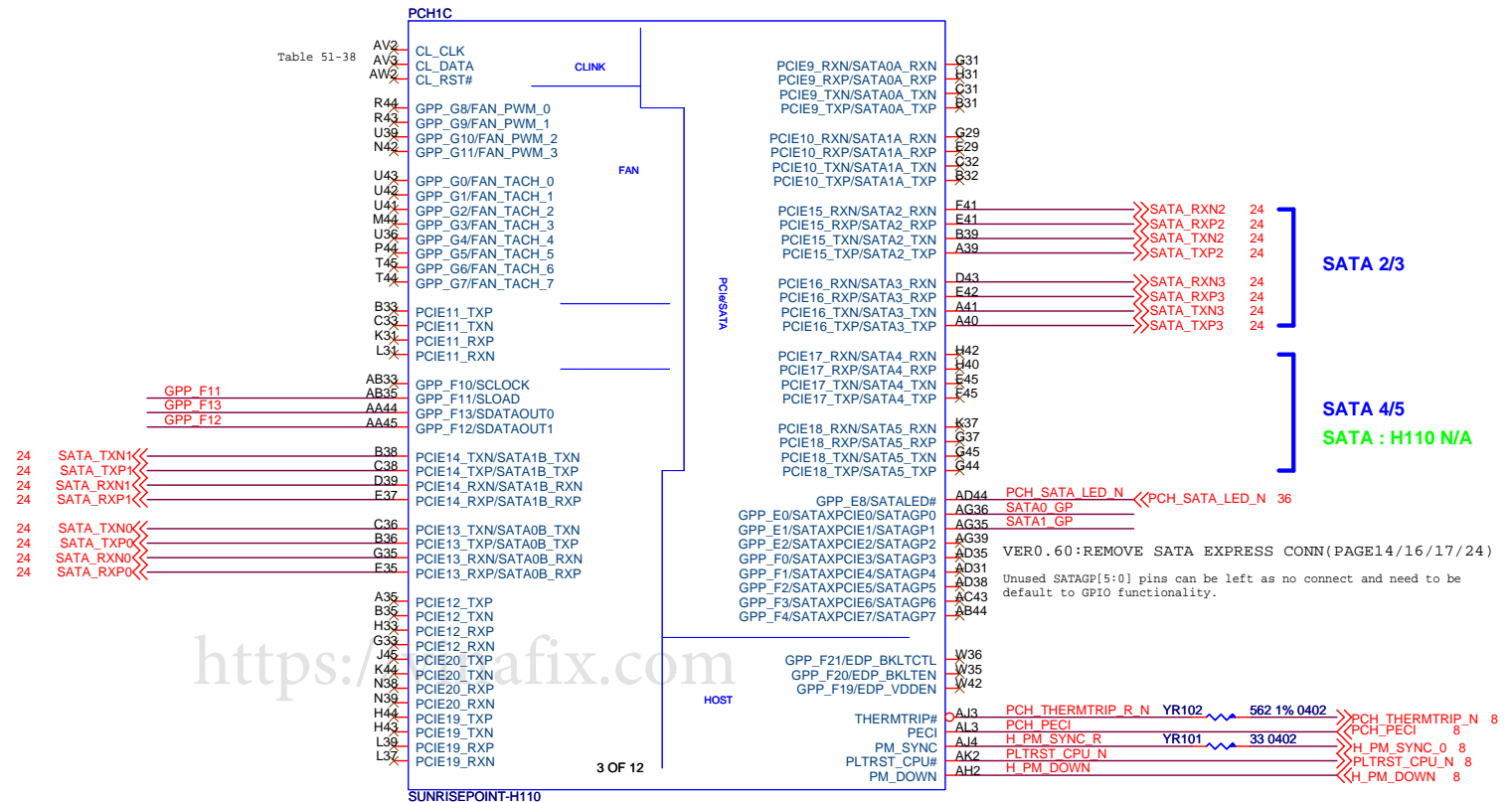
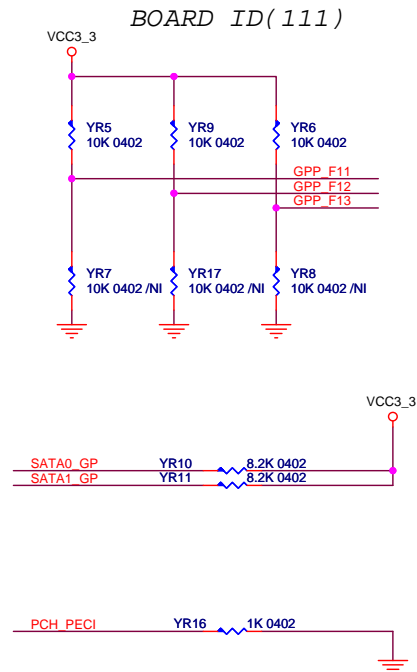
PCH PART: Y+Reference

[illegible]

Vinafix.com



PCH PART: Y+Reference



GbE can be mapped into one of the PCIe Ports 4-5, Port 9, and Ports 12-13.

◆ BIOSTAR'S PROPRIETARY INFORMATION ◆

◆ Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties. ◆

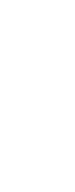
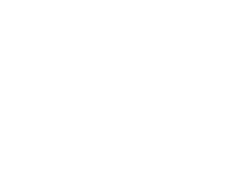
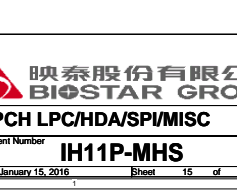
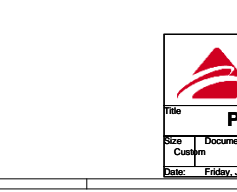
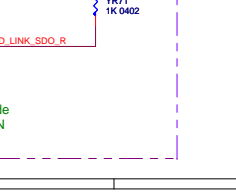
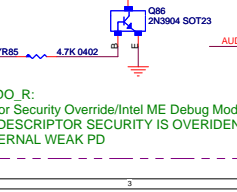
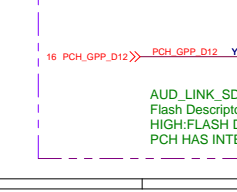
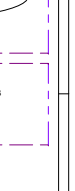
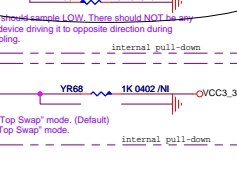
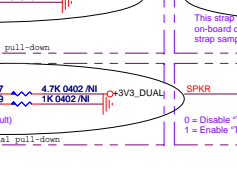
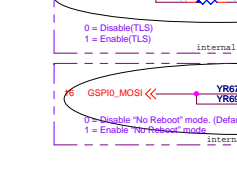
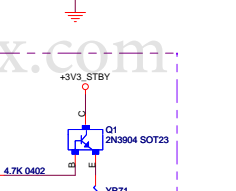
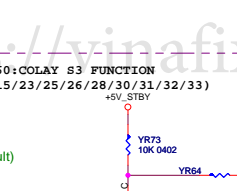
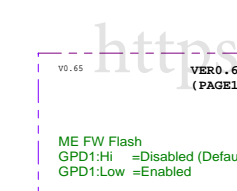
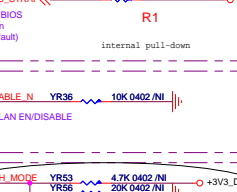
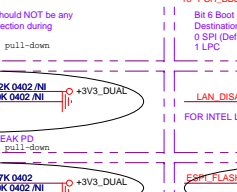
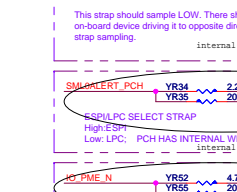
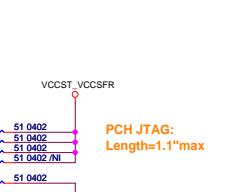
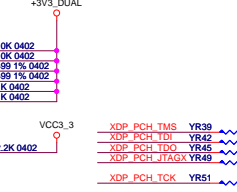
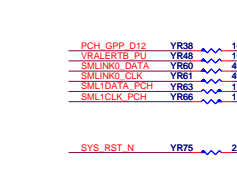
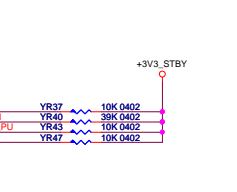
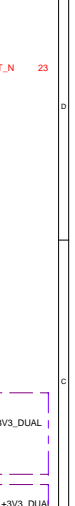
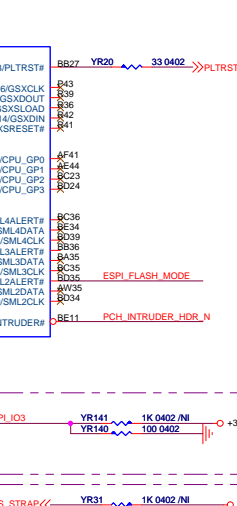
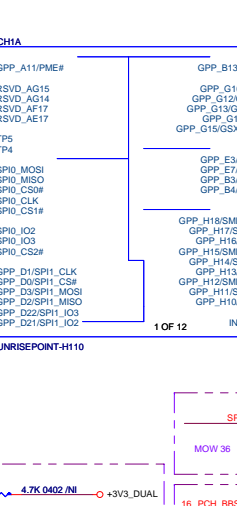
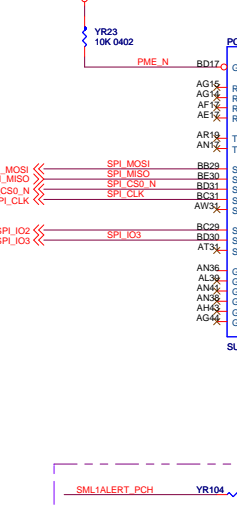
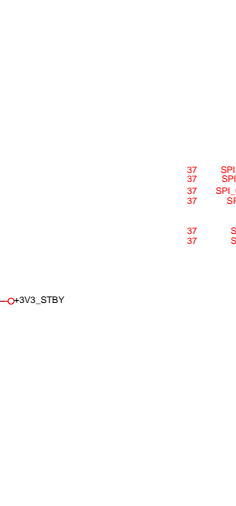
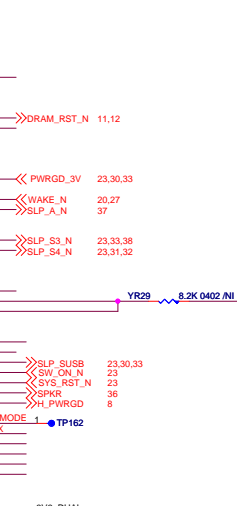
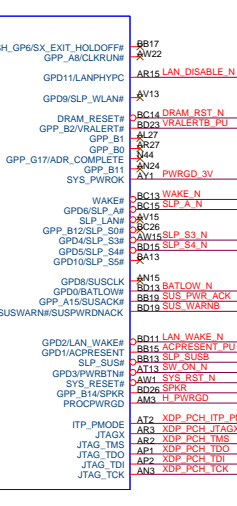
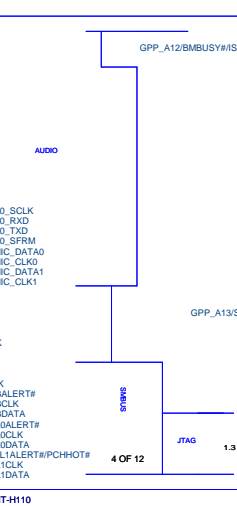
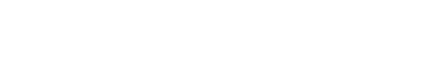
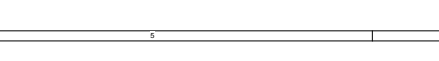
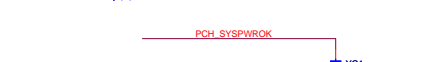
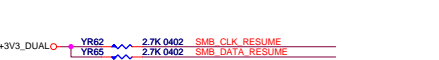
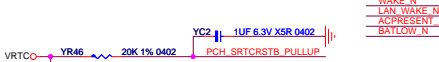
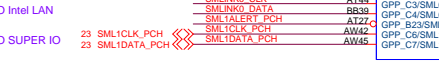
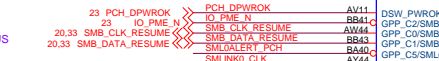
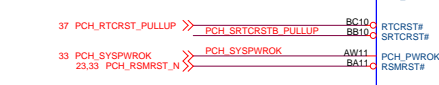
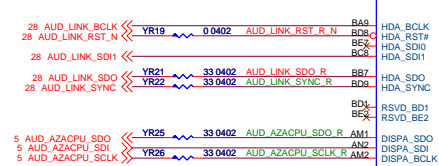


Title PCH CLINK/SATA/CPU HOST

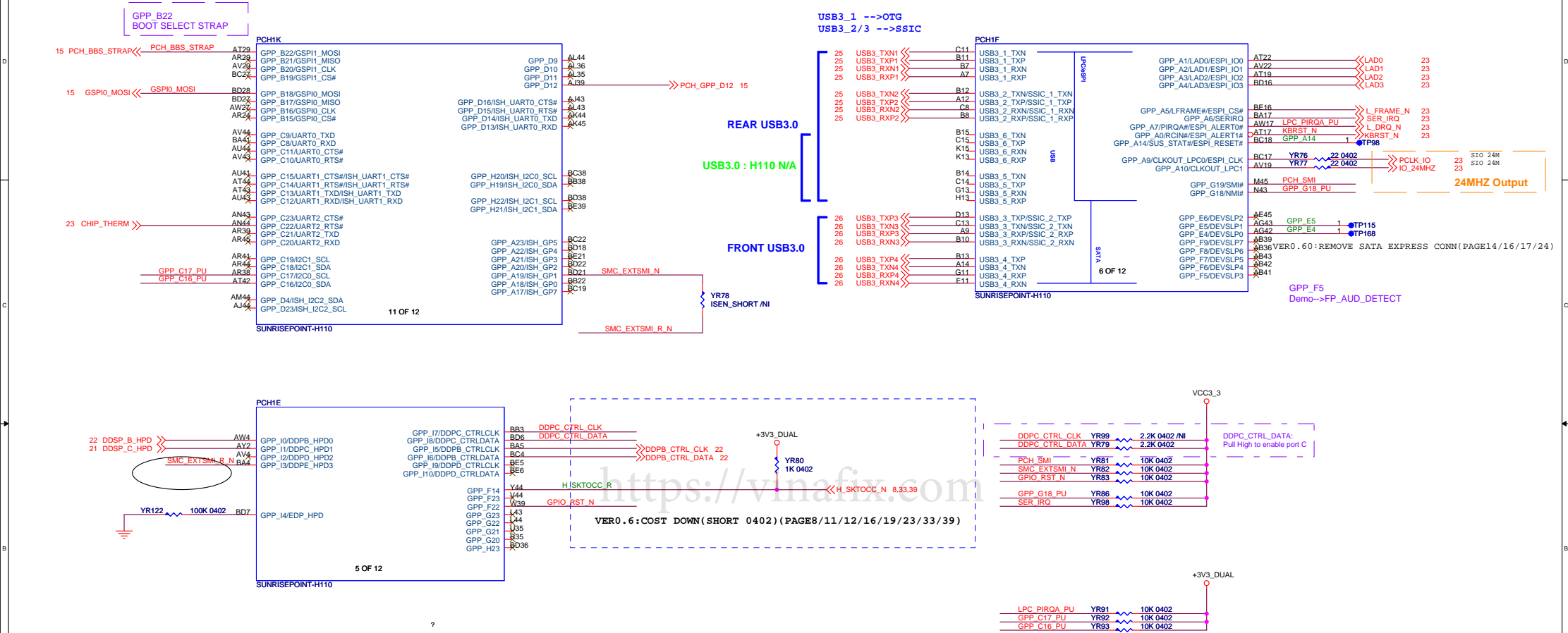
Size B Document Number IH11P-MHS Rev 6.0

Date: Friday, January 15, 2016 Sheet 14 of 42

HDA_SDO and HDA_BCLK matched within 500mils



PCH PART: Y+Reference



Vinafix.com

BIOS/STAR'S PROPRIETARY INFORMATION

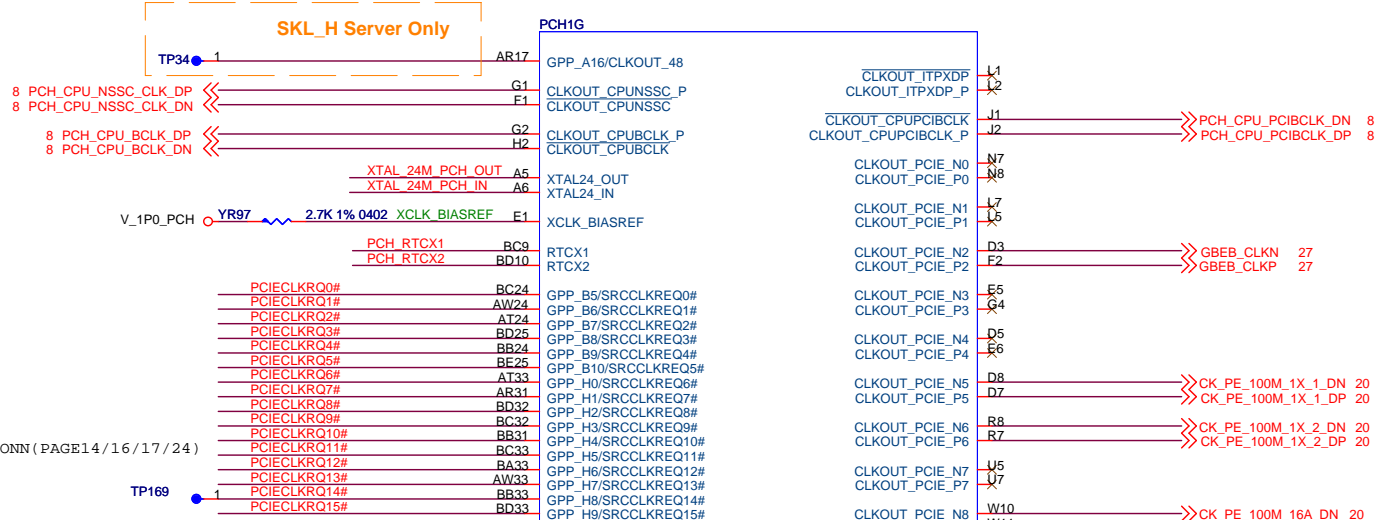
Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties.

映泰股份有限公司
BIOS/STAR GROUP

Title: **PCH LPC/DP/USB3/UART**

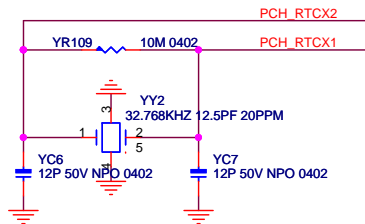
Size: Custom Document Number: **IH11P-MHS** Rev: 6.0


Date: Friday, January 15, 2016 Sheet: 16 of 42

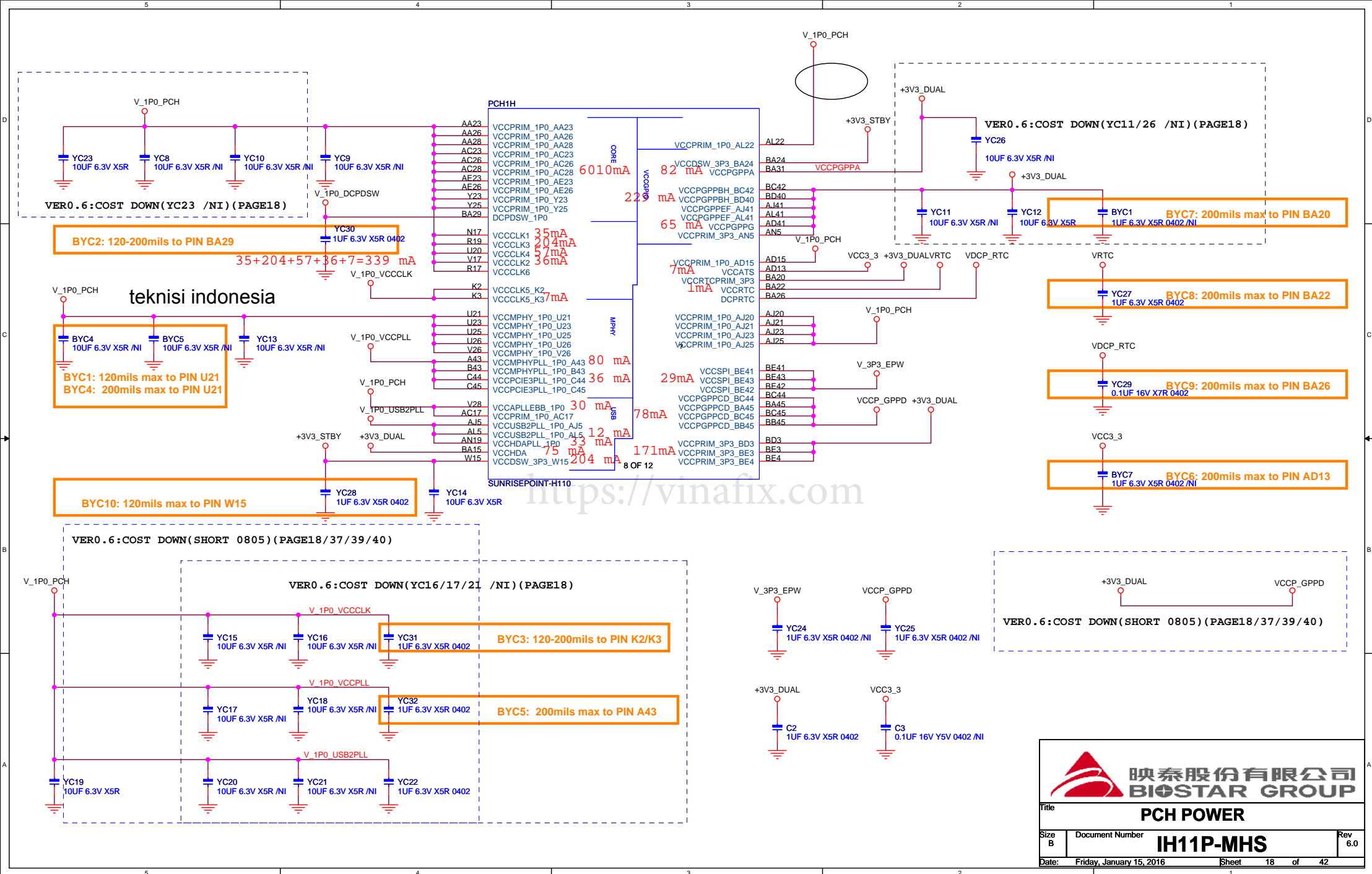


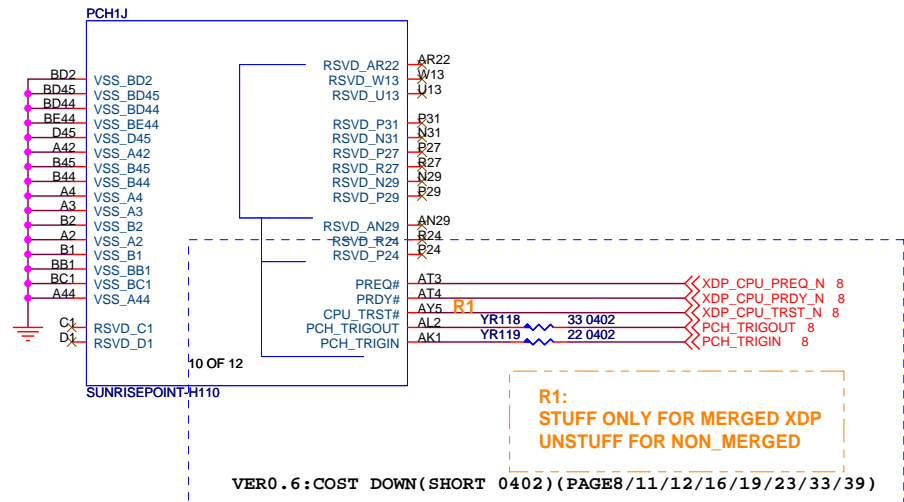
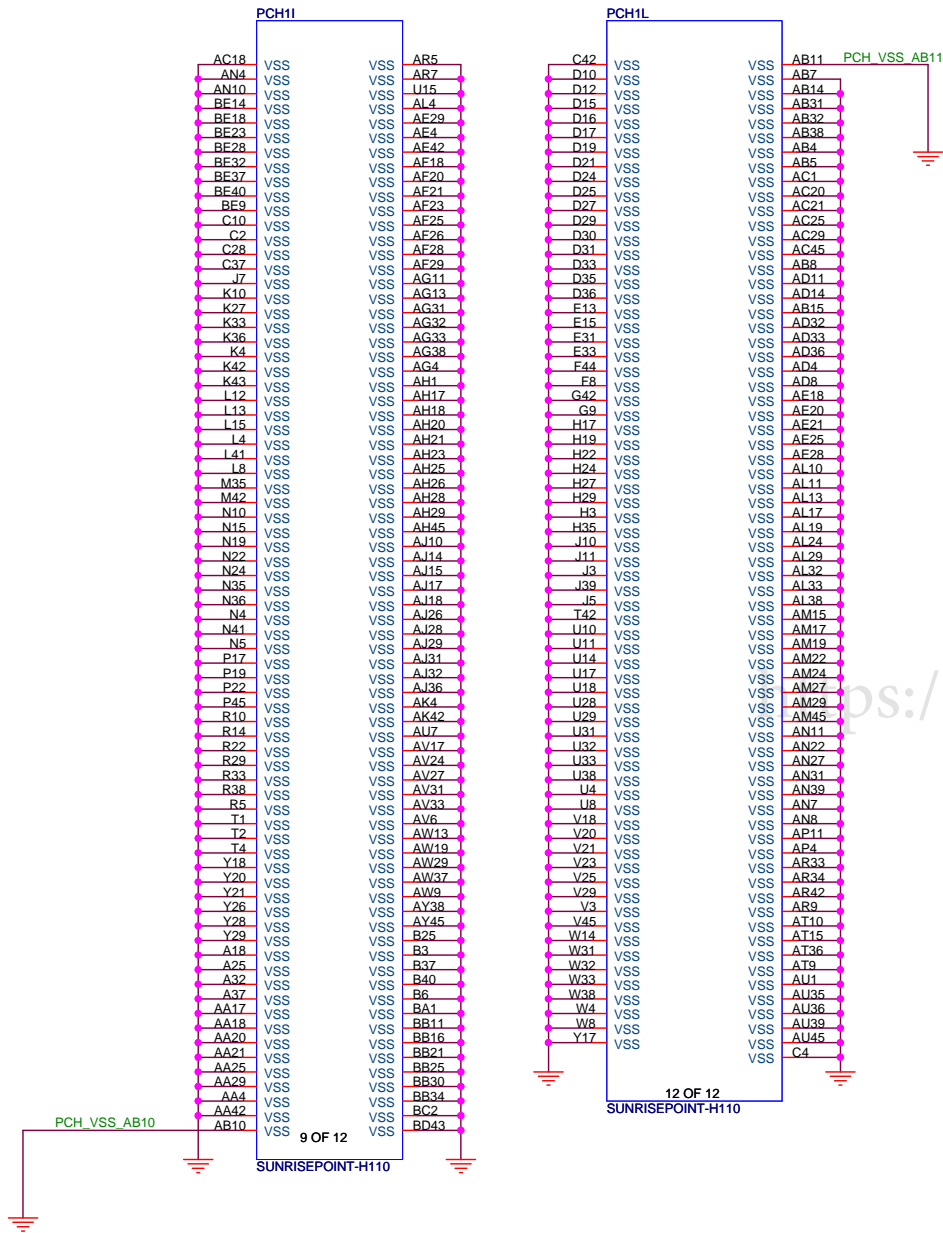
VER0.60:REMOVE SATA EXPRESS CONN(PAGE14/16/17/24)

PTC CRYSTAL



	
PCH CLOCK BUFFER	
Title	Document Number
Size B	IH11P-MHS
Date: Friday, January 15, 2016	Sheet 17 of 42
Rev 6.0	



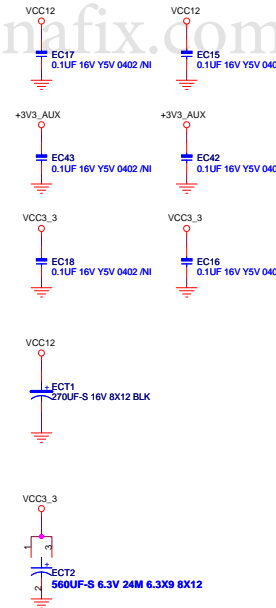
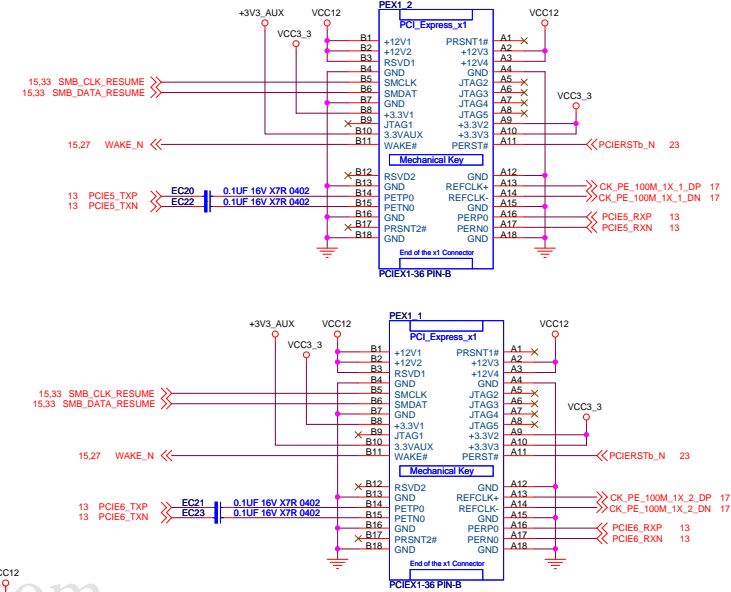
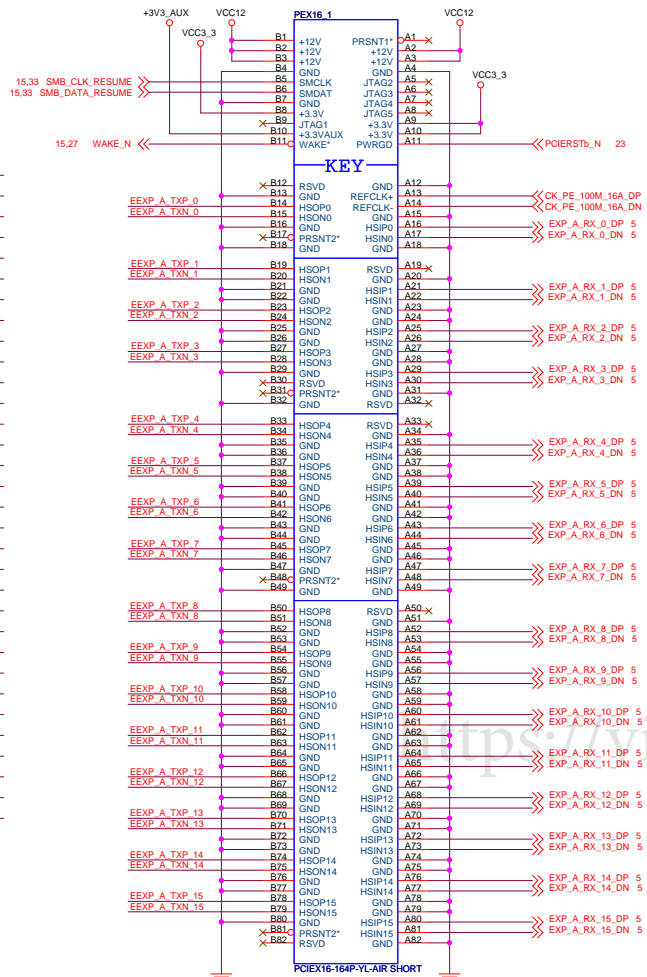


SLOT PART: E+Reference

Vinafix.com

Value:180 nF - 265 nF

450 mils max to connector pin

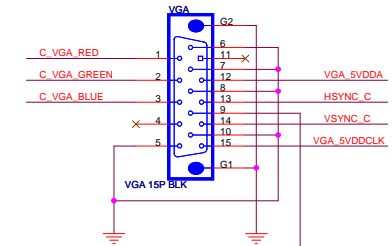
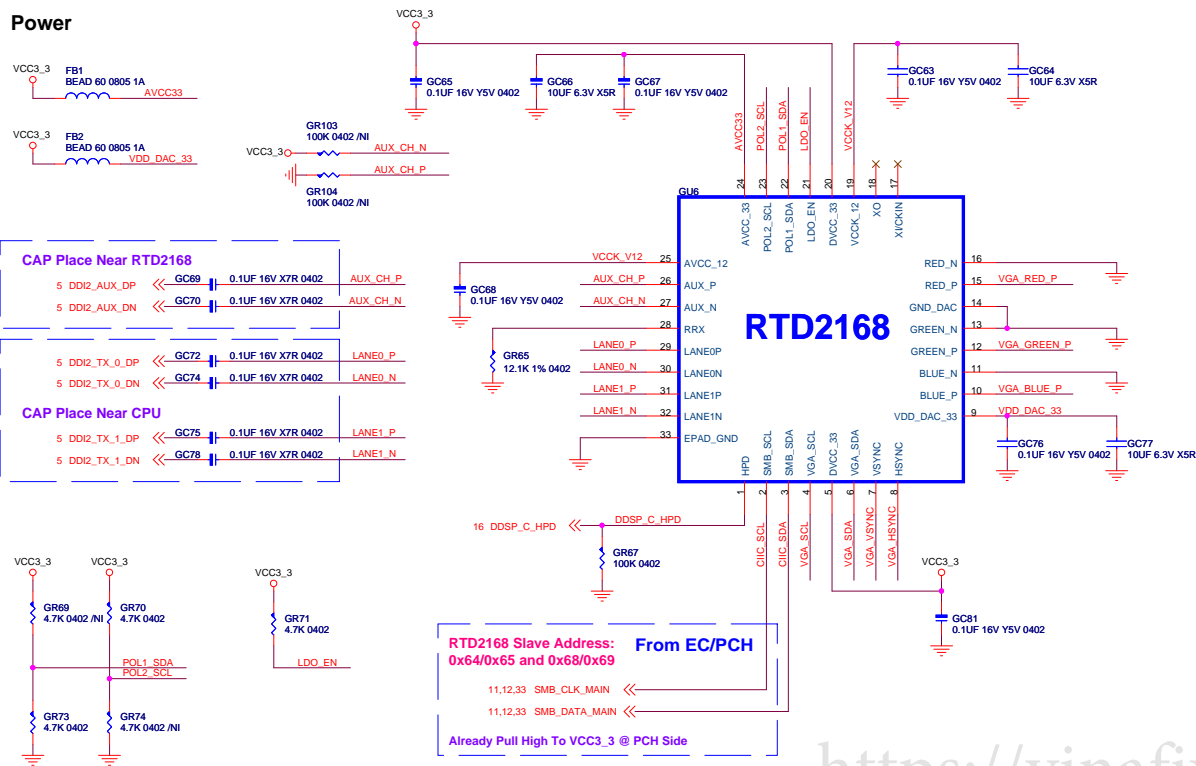


BIOSTAR'S PROPRIETARY INFORMATION

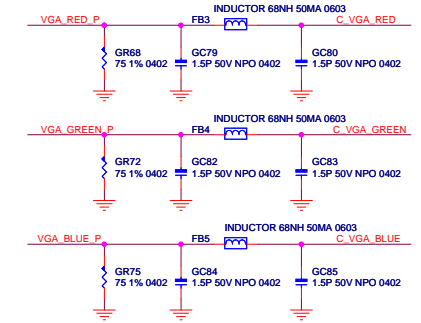
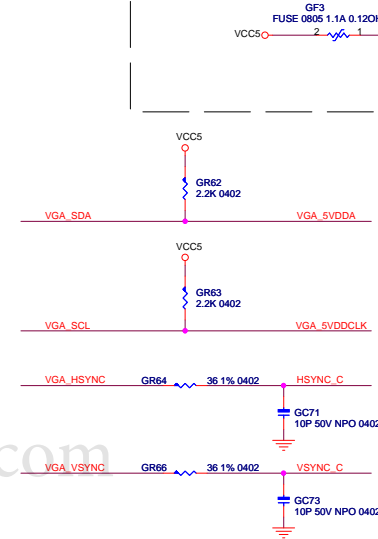
Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties.

 映泰股份有限公司 BIOSTAR GROUP	
PCIEX16 SLOT 1 & 2	
Title PCIE16-SLOT 1 & 2	Document Number IH11P-MHS
Date: Friday, January 15, 2016	Sheet 20 of 42

Power



VER0.6:COST DOWN(MODIFY F6/GF3 SIZE)(PAGE21/34)



Mode Configure Table(Power On Latch)

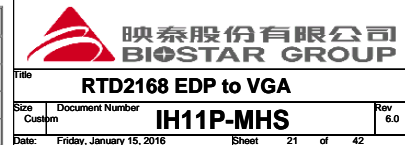
		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EPPROM MODE

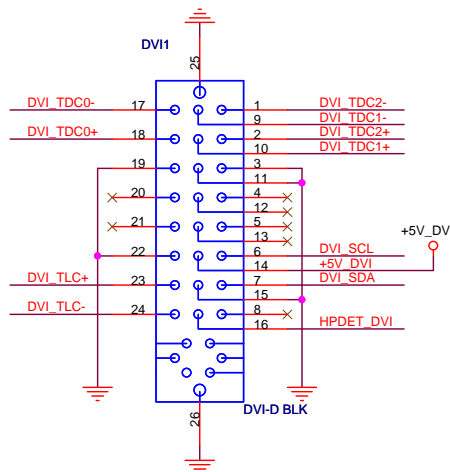
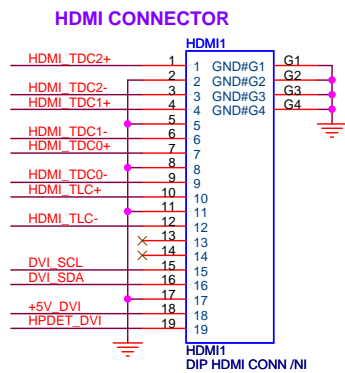
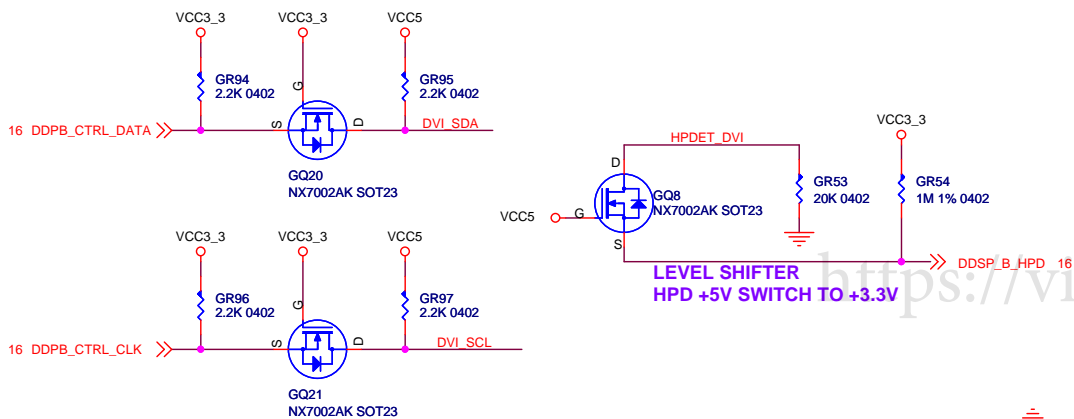
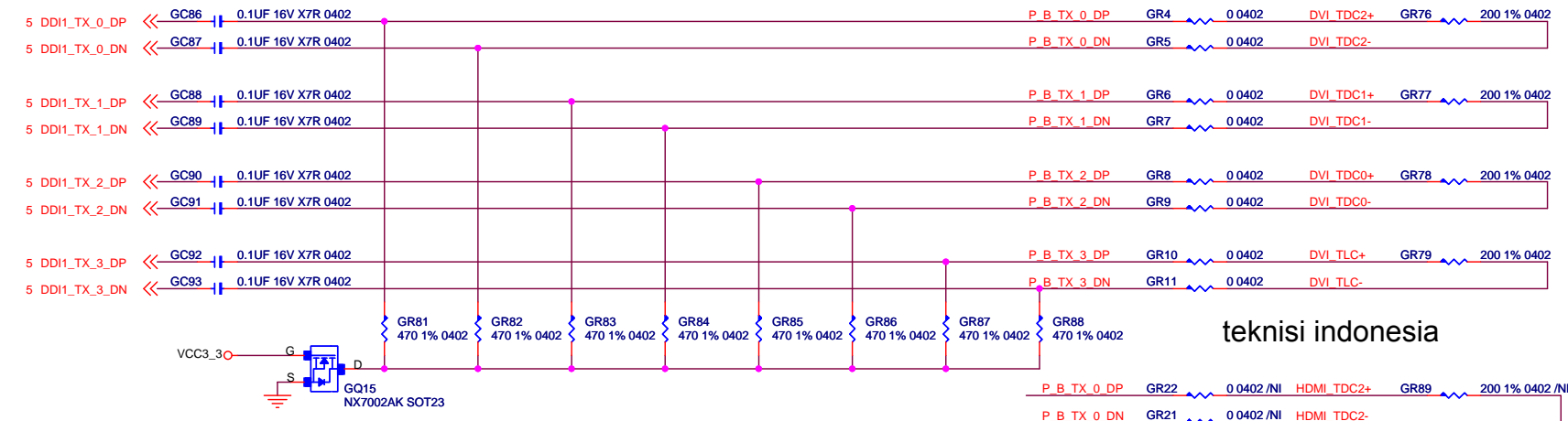
Embedded LDO

LDO_EN(PIN21)	
0	1
VCCCK_V12 from External 1.2V	VCCCK_V12 from Embedded LDO

Table 12 Power consumption by using embedded LDO and embedded clock source

Active Resolution / Standby	DP Config.	Min	Typ	Max	Unit
1280x800x60(74.25-MHz)	1-Lane	-	400	450	mW
1600x900x60(103-MHz)	1-Lane	-	420	480	mW
1920x1080x60(148-MHz)	2-Lane	-	480	595	mW
Stand-by mode	-	-	7.5	8	mW





◆ BIOSTAR'S PROPRIETARY INFORMATION ◆

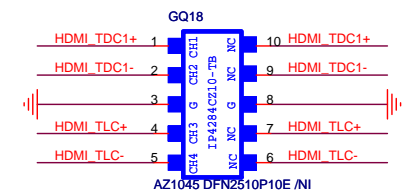
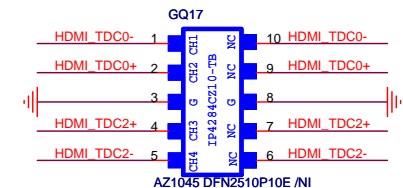
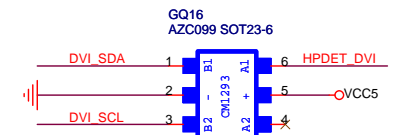
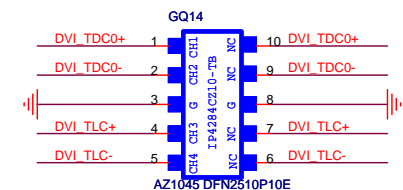
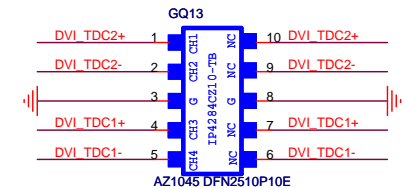
◆ Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties. ◆

映泰股份有限公司
BIOSTAR GROUP

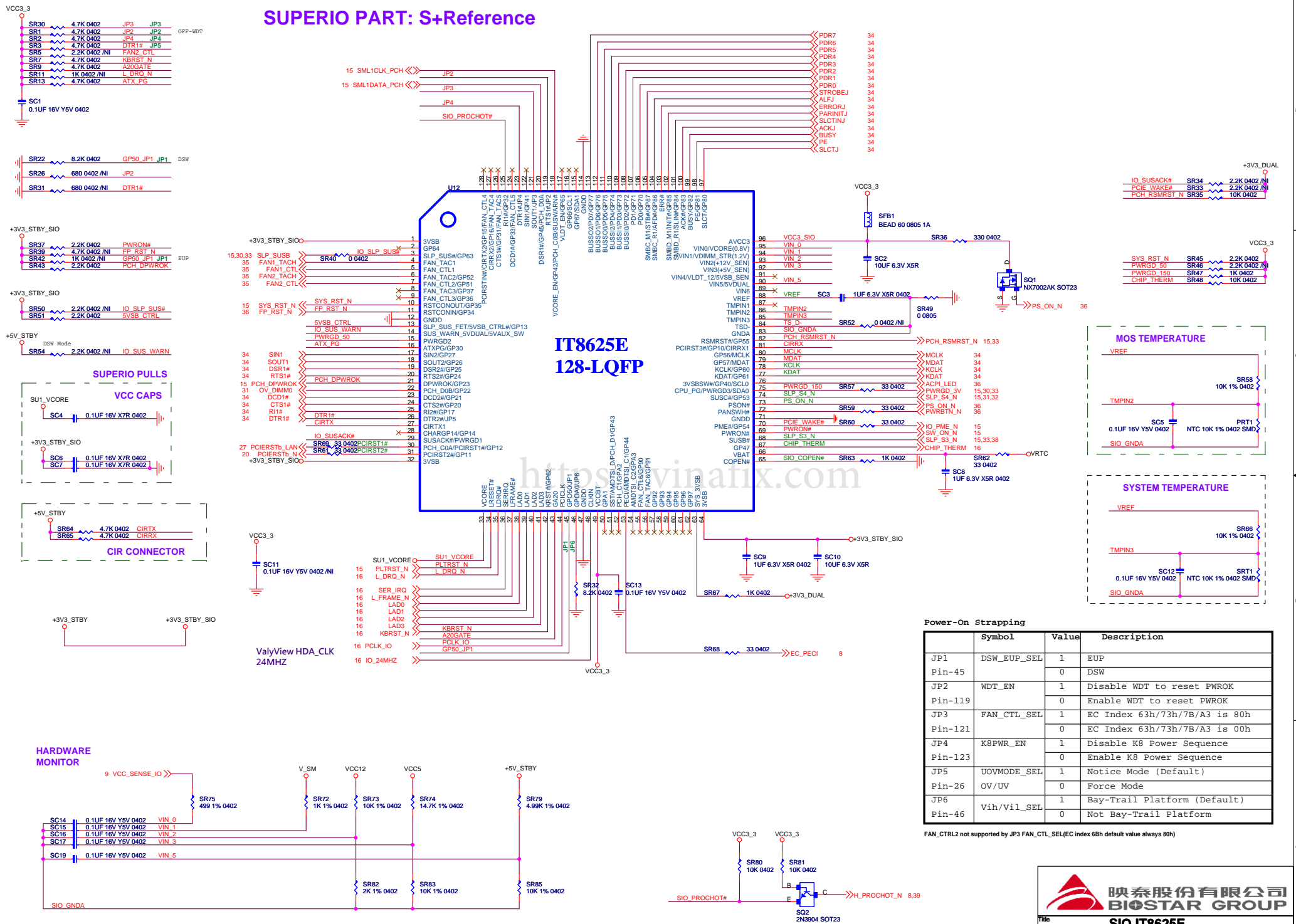
Title **DVI-I CONNECTOR**

Size B Document Number **IH11P-MHS** Rev 6.0

Date: Friday, January 15, 2016 Sheet 22 of 42




SUPERIO PART: S+Reference



Power-On Strapping

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin-45		0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-119		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 63h/73h/7B/A3 is 80h
Pin-121		0	EC Index 63h/73h/7B/A3 is 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence
Pin-123		0	Enable K8 Power Sequence
JP5	UOVMODE_SEL	1	Notice Mode (Default)
Pin-26	OV/UV	0	Force Mode
JP6	Vih/Vil_SEL	1	Bay-Trail Platform (Default)
Pin-46		0	Not Bay-Trail Platform

FAN_CTRL2 not supported by JP3 FAN_CTL_SEL/EC index 6Bh default value always 80h)



映泰股份有限公司
BIOSTAR GROUP

Title

SIO IT8625E

Size

Document Number

IH11P-MHS

Rev

6.0

Date

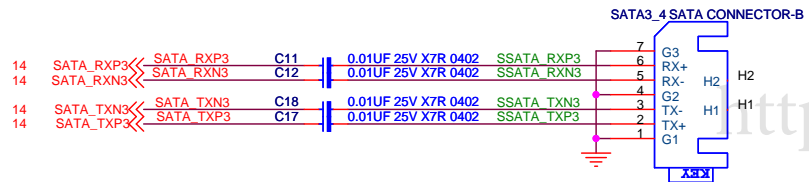
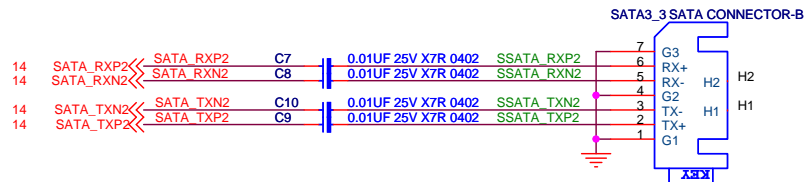
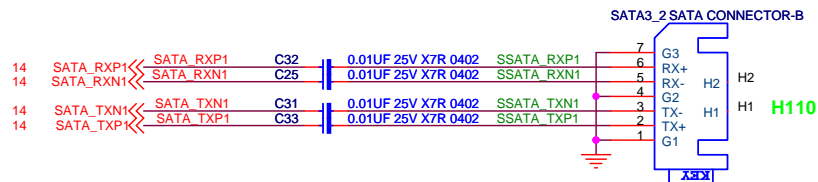
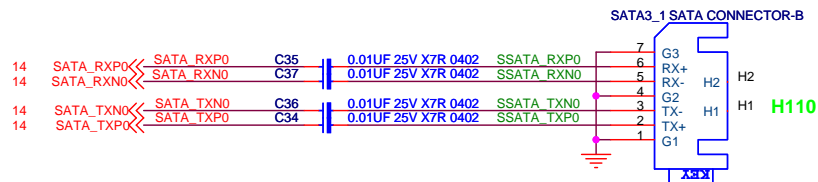
Friday, January 15, 2016

Sheet

23


of

48

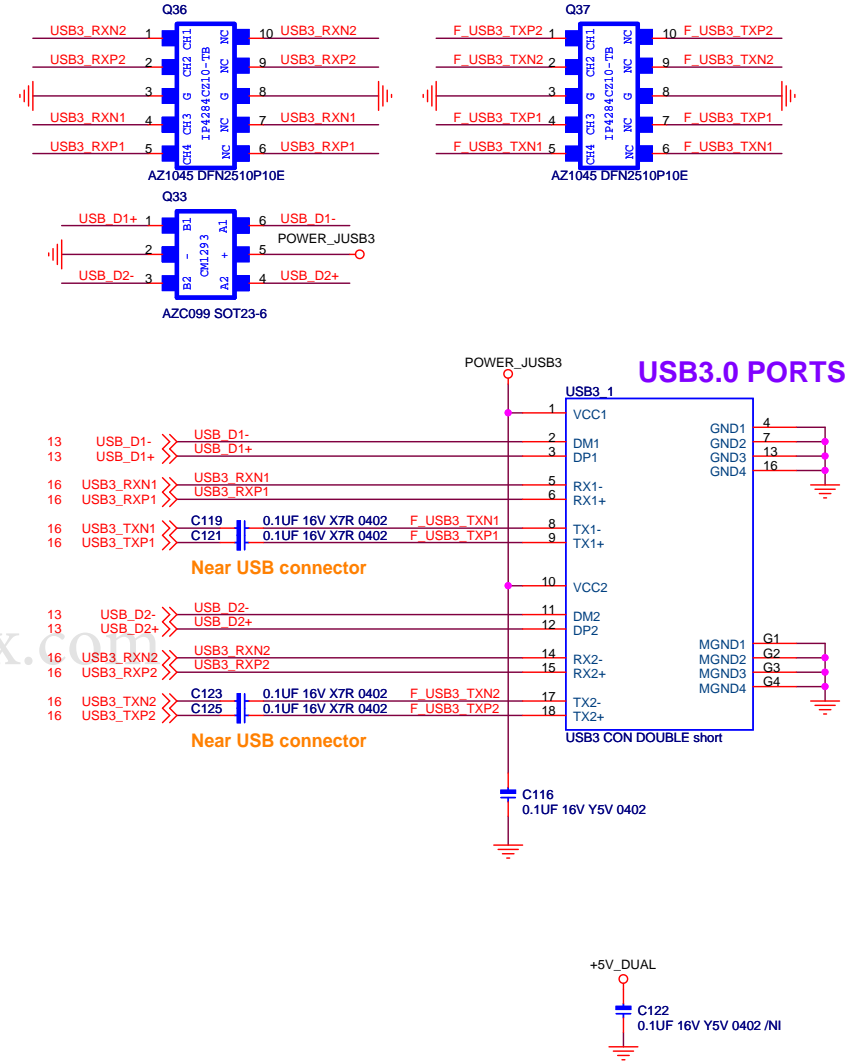
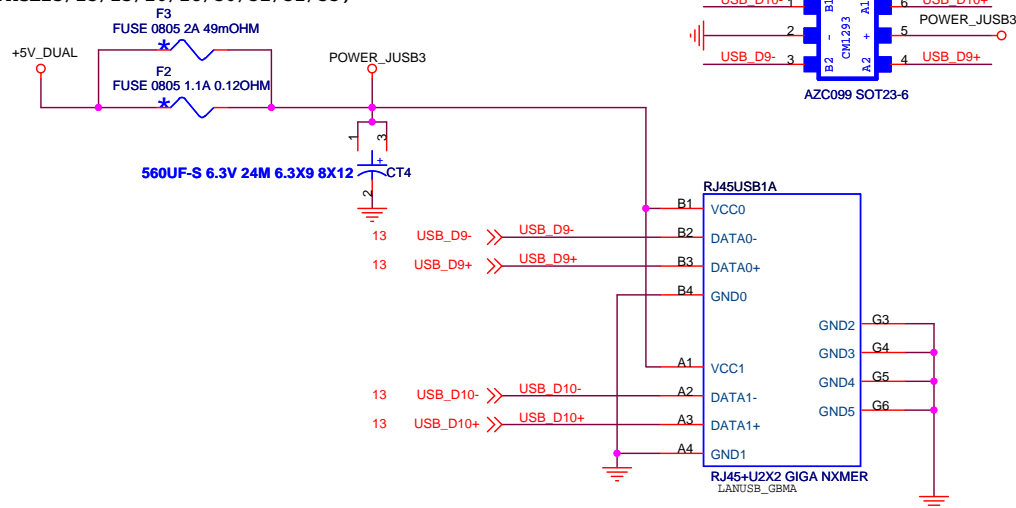


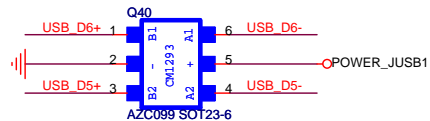
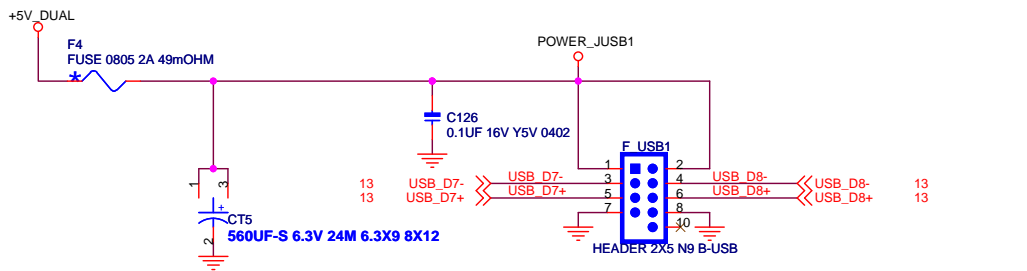
Vinafix.com

https://vinafix.com

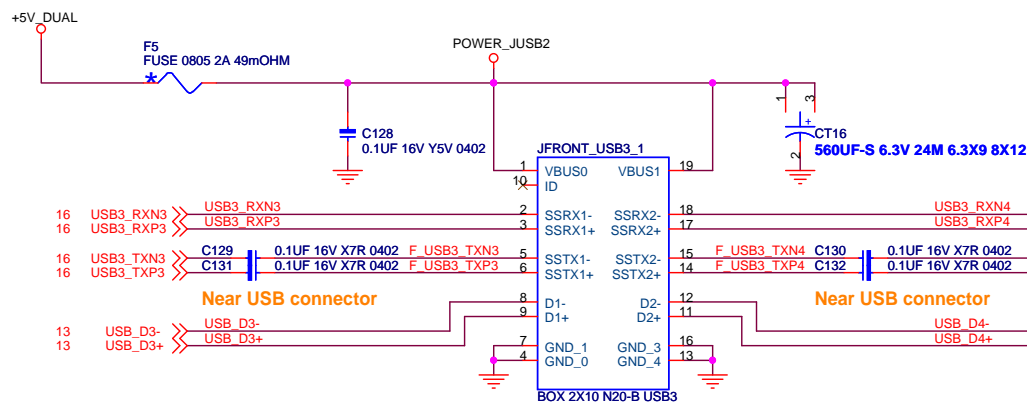
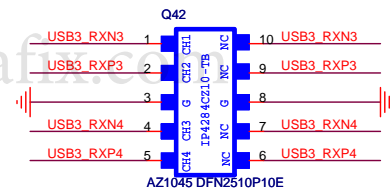
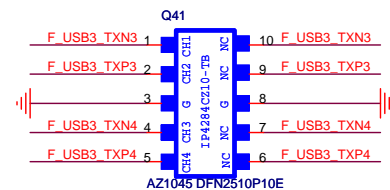
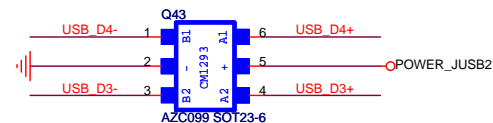
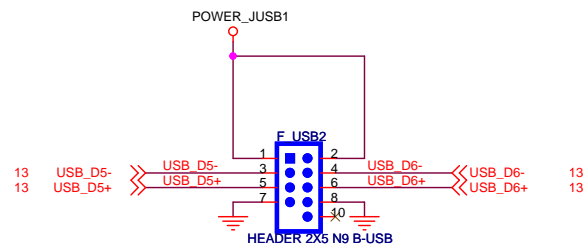
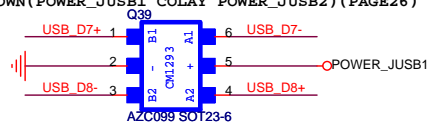
 映泰股份有限公司 BIOSTAR GROUP			
Title SATA EXPRESS			
Size B	Document Number IH11P-MHS		Rev 6.0
Date: Friday, January 15, 2016		Sheet 24 of 42	

VER0.60:COLAY S3 FUNCTION
(PAGE15/23/25/26/28/30/31/32/33)






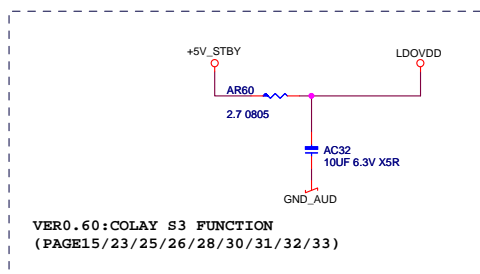
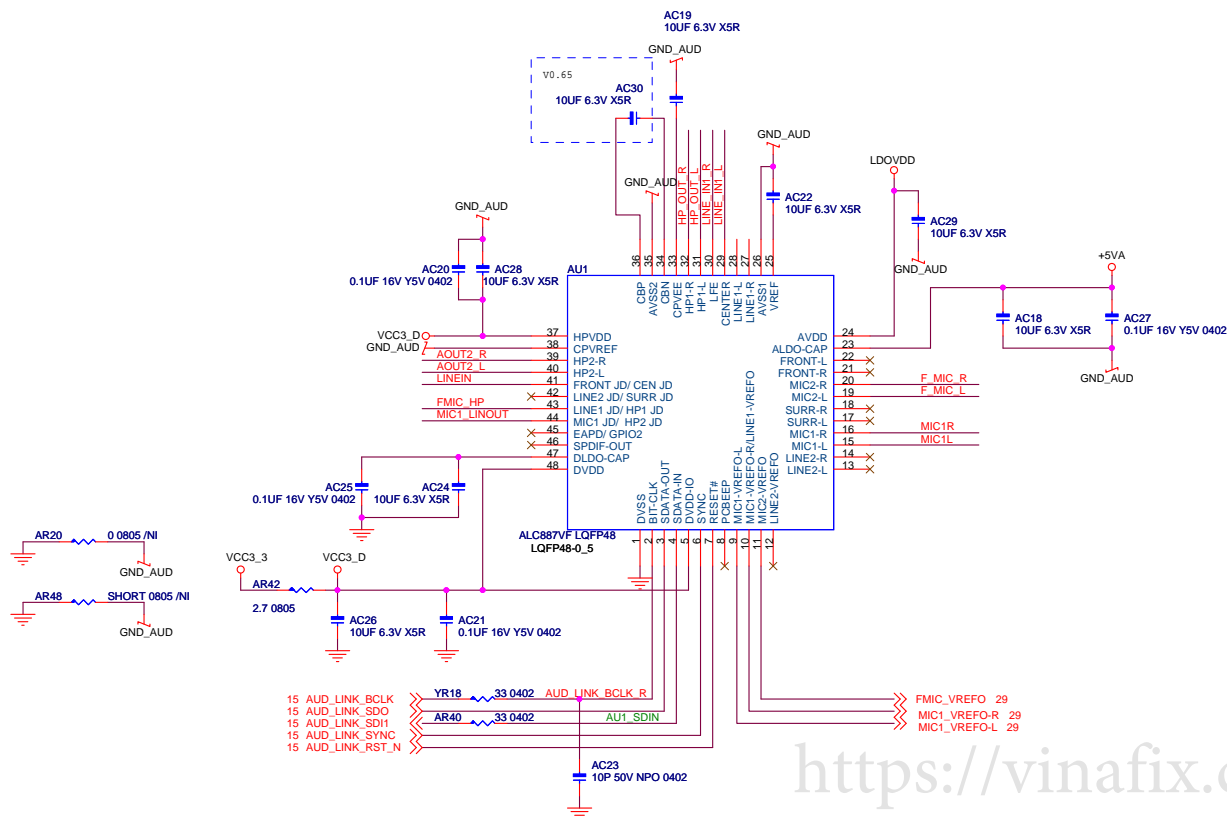
VER0.6: COST DOWN (POWER_JUSB1, COLAY, POWER_JUSB2) (PAGE26)



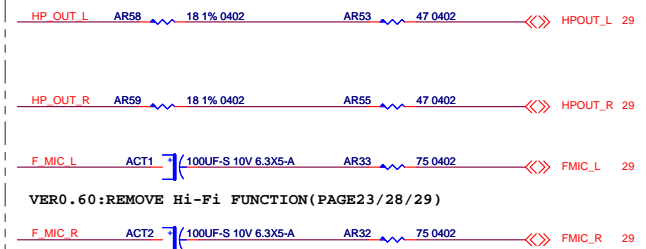
❖ BIOSTAR'S PROPRIETARY INFORMATION ❖

❖ Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties. ❖

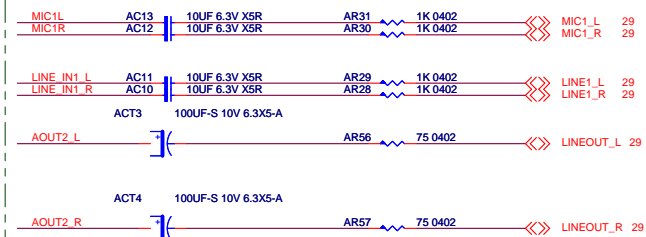
 映泰股份有限公司 BIOSTAR GROUP		FRONT USB IH11P-MHS	
Size	Document Number	Date:	Rev
B		Friday, January 15, 2016	6.0
Sheet		of	
26		42	



FRONT CHANNEL

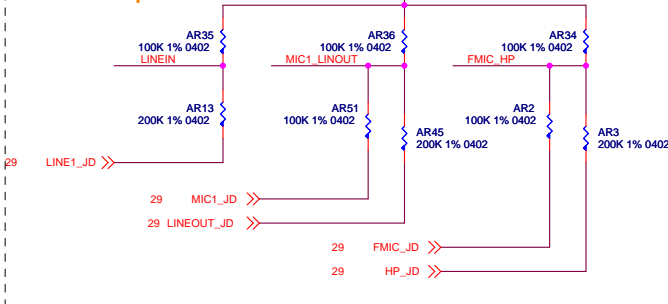


REAR CHANNEL



JD Group

as close as possible to AU1



◆BIOSTAR'S PROPRIETARY INFORMATION◆

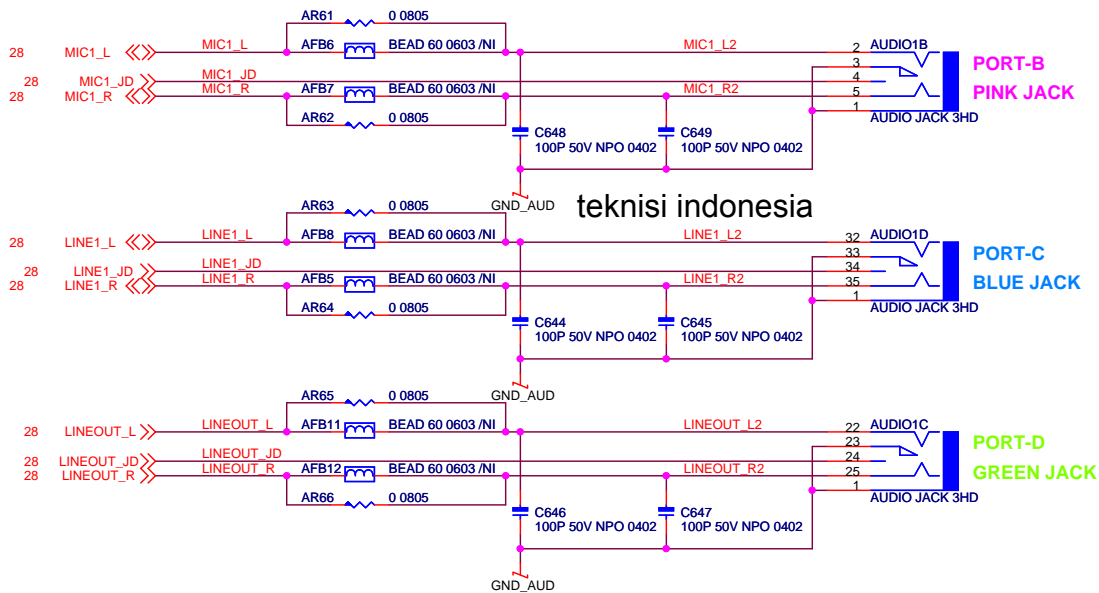
◆Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties.◆

映泰股份有限公司
BIOSTAR GROUP

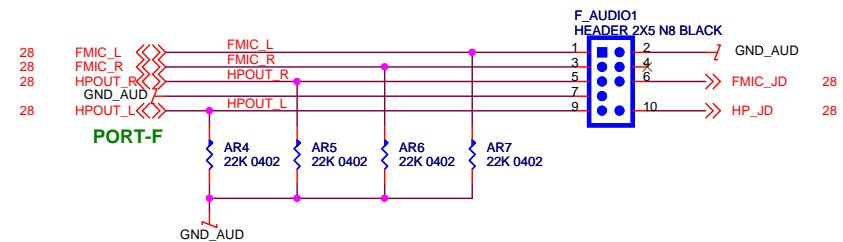
Title: **AUDIO CODEC ALC887**

Size: Custom Document Number: **IH11P-MHS** Rev: 6.0

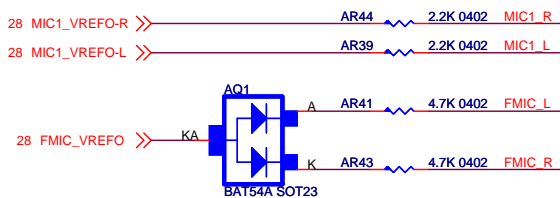
Date: Friday, January 15, 2016 Sheet 28 of 42



FRONT AUDIO HEADER



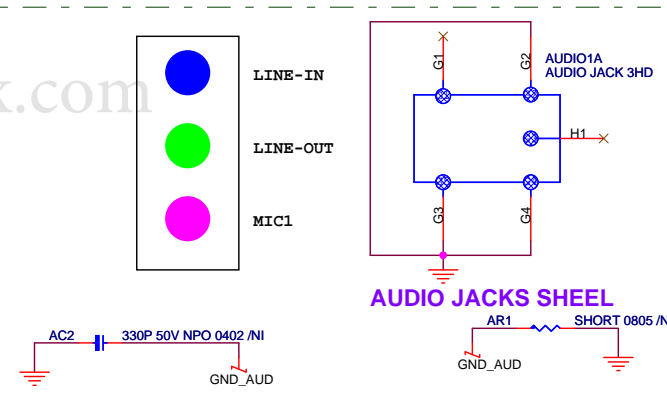
MIC VREF



SPDIF CONNECTOR

V0.66

<https://vinafix.com>



◇ BIOSTAR'S PROPRIETARY INFORMATION ◇

◇ Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties. ◇

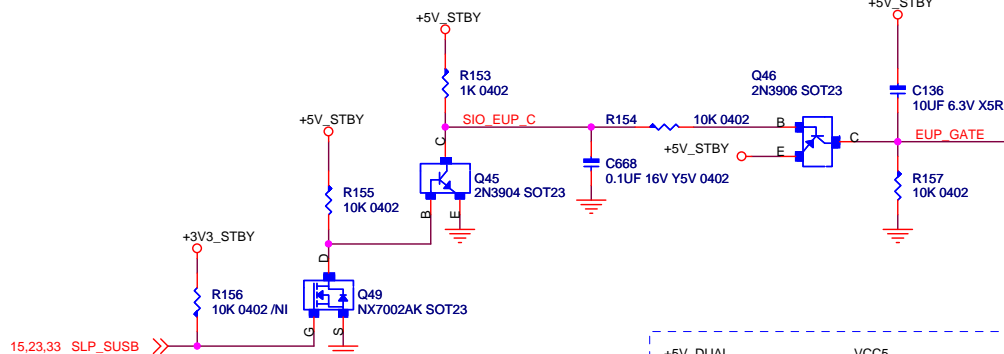


映泰股份有限公司
BIOSAR GROUP

Title
AUDIO CONNECTOR

Size B Document Number
IH11P-MHS Rev 6.0

Date: Friday, January 15, 2016 Sheet 29 of 42

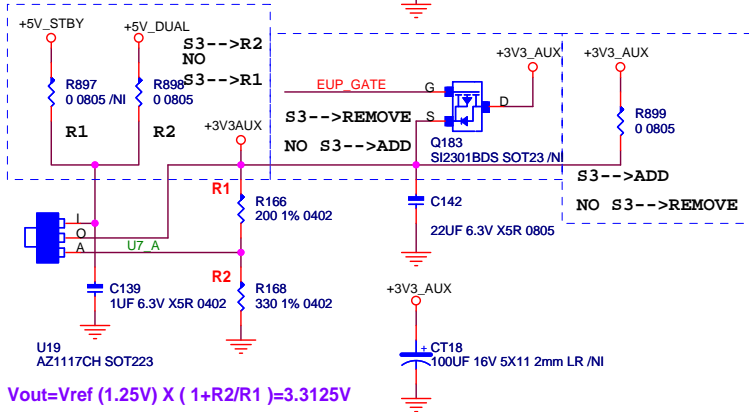
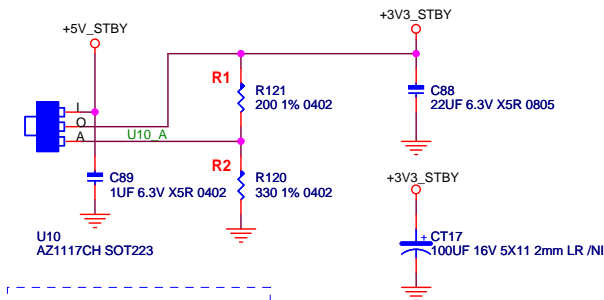


Energy-Using Product(EUP)

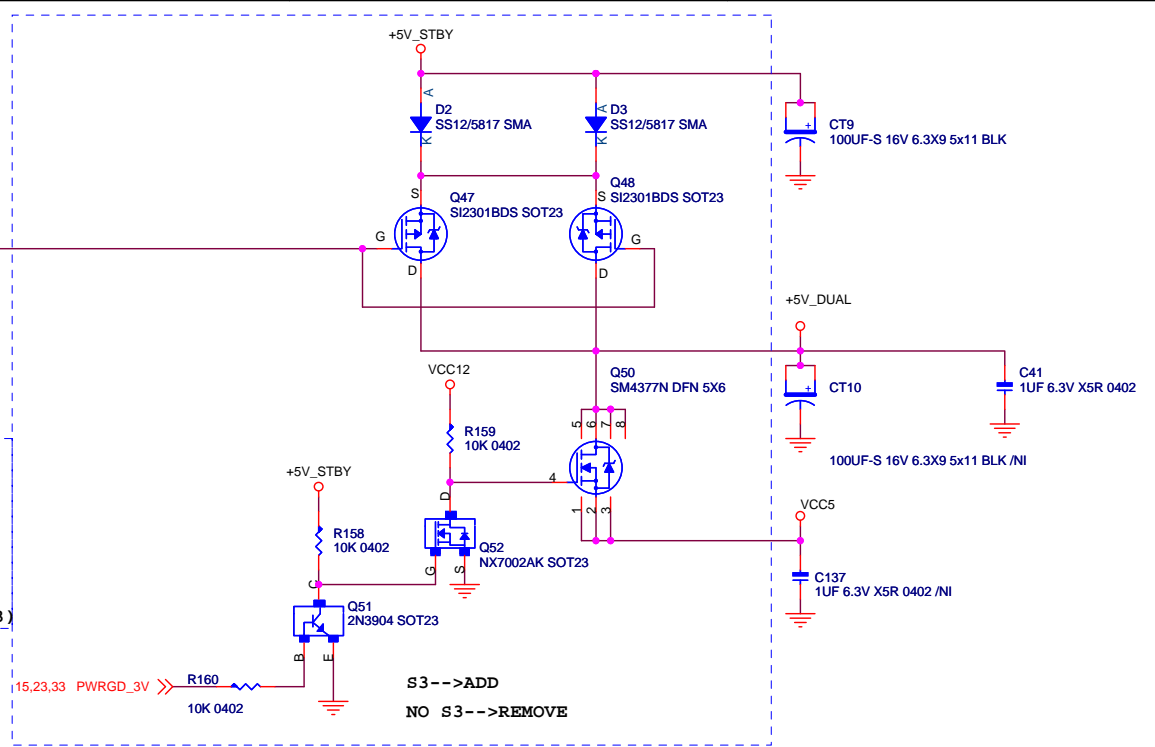
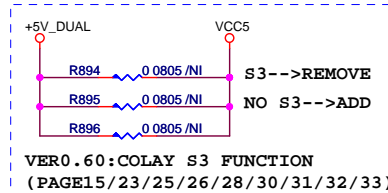
SLP_SUSB Hight :EUP OFF

SLP_SUSB Low :EUP ON

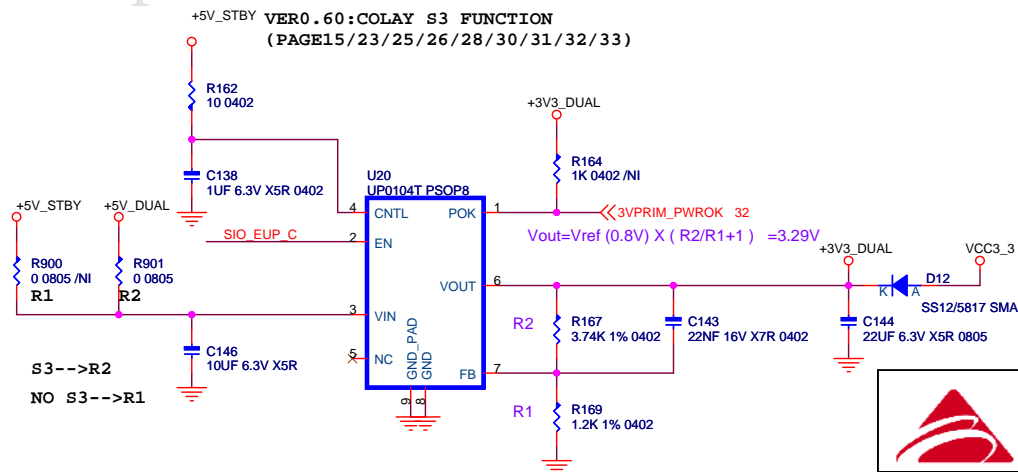
$$V_{out} = V_{ref} (1.25V) \times (1 + R2/R1) = 3.3125V$$




$$V_{out} = V_{ref} (1.25V) \times (1 + R2/R1) = 3.3125V$$

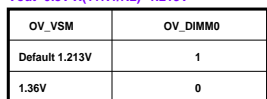


<https://vinafix.com>

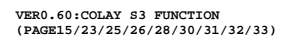
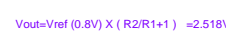


 映泰股份有限公司 BIOSSTAR GROUP	
Title ACPI POWER	
Size B	Document Number IH11P-MHS
Date: Friday, January 15, 2016	Rev 6.0
Sheet 30	of 42

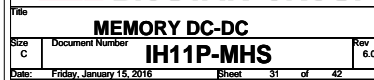
VER0.60:COLAY S3 FUNCTION
(PAGE15/23/25/26/28/30/31/32/33)

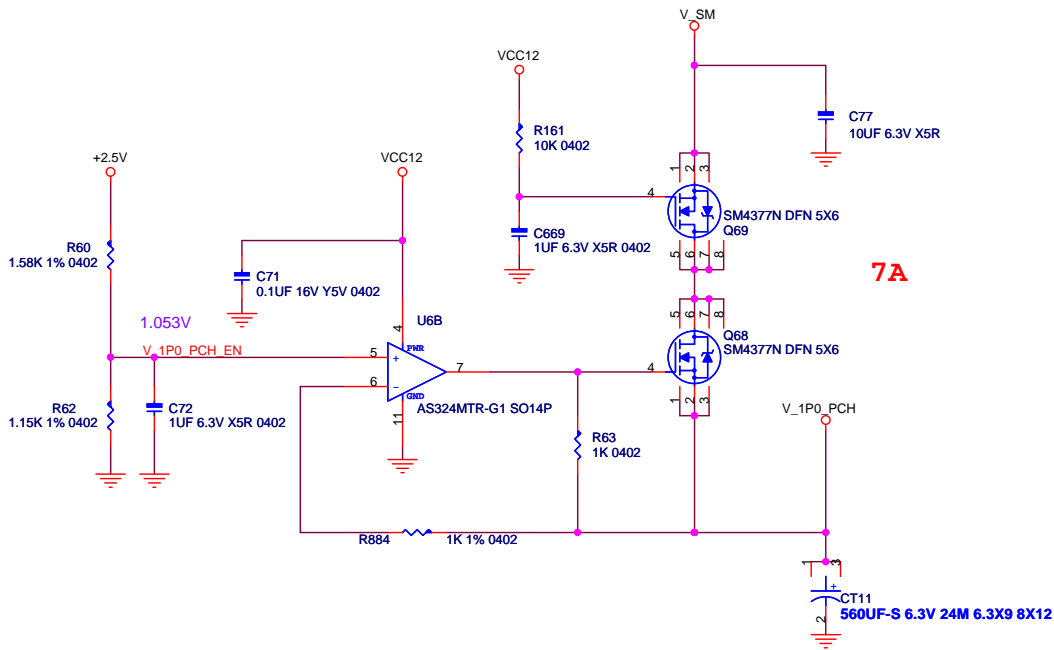


VER0.6:COST DOWN(MCT2/3/CT11 CHANGE TO 560UF)(PAGE31/32)



◆Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties.◆

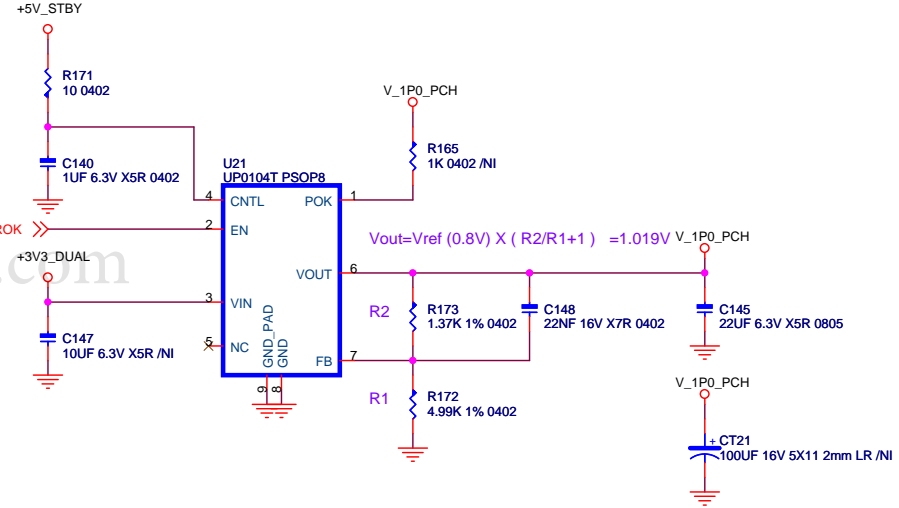




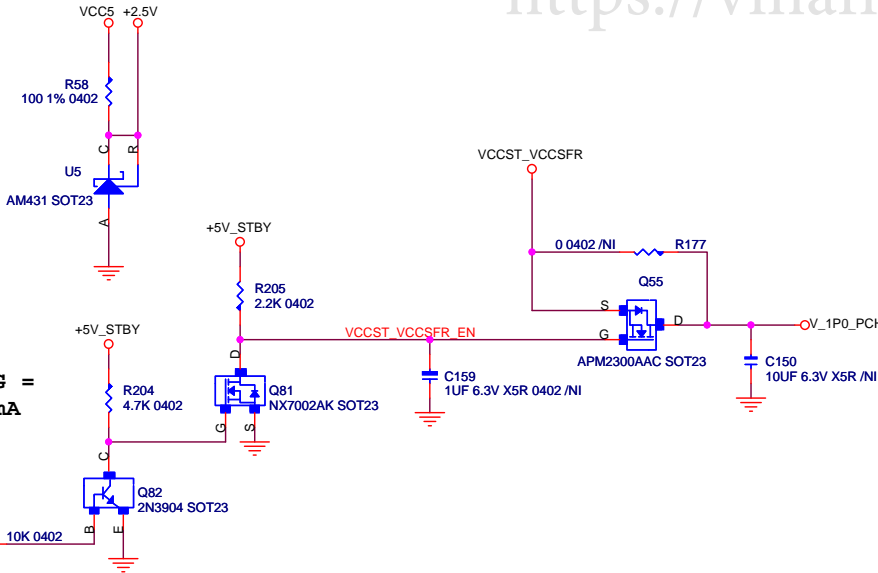
7A

Vinafix.com

<https://vinafix.com>



$$V_{out} = V_{ref} (0.8V) \times \left(\frac{R_2}{R_1 + 1} \right) = 1.019V \quad V_{1P0_PCH}$$



$$VCCST + VCCSTG = 0.06 + 0.06 \text{ mA}$$

BIOSTAR'S PROPRIETARY INFORMATION

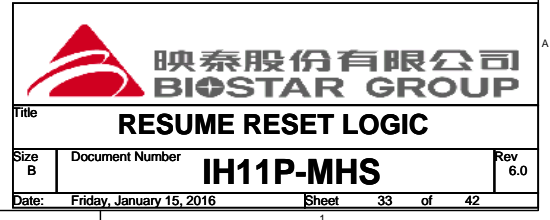
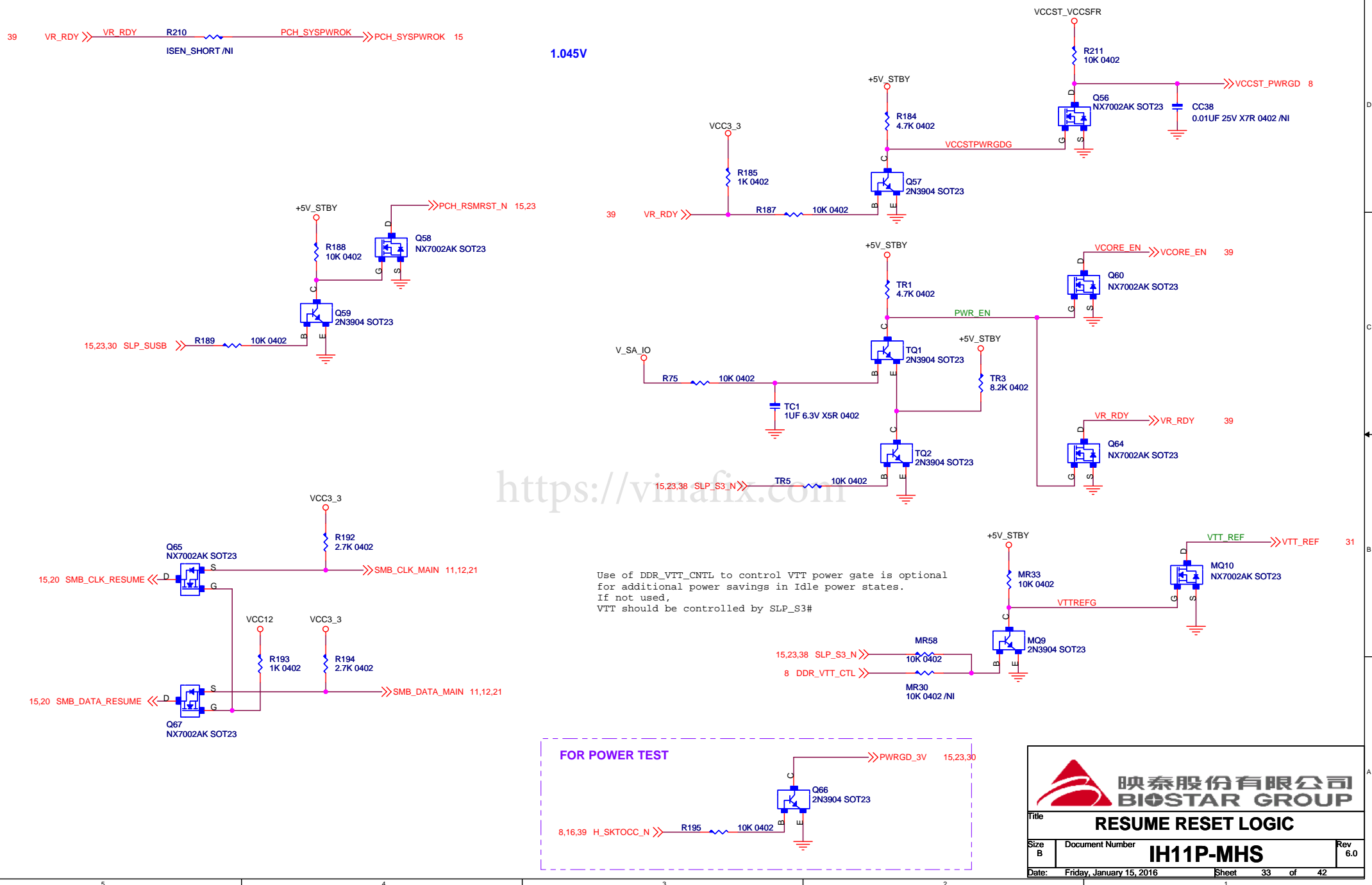
Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties.

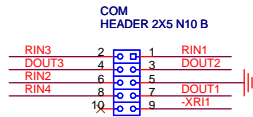
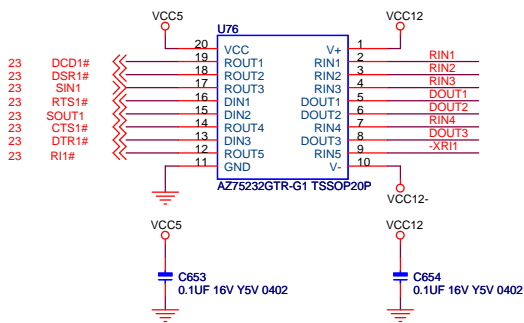
映泰股份有限公司
BIOSTAR GROUP

V_1P0_PCH

IH11P-MHS

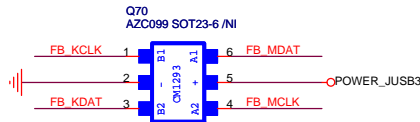
Date: Friday, January 15, 2016 Sheet 32 of 42



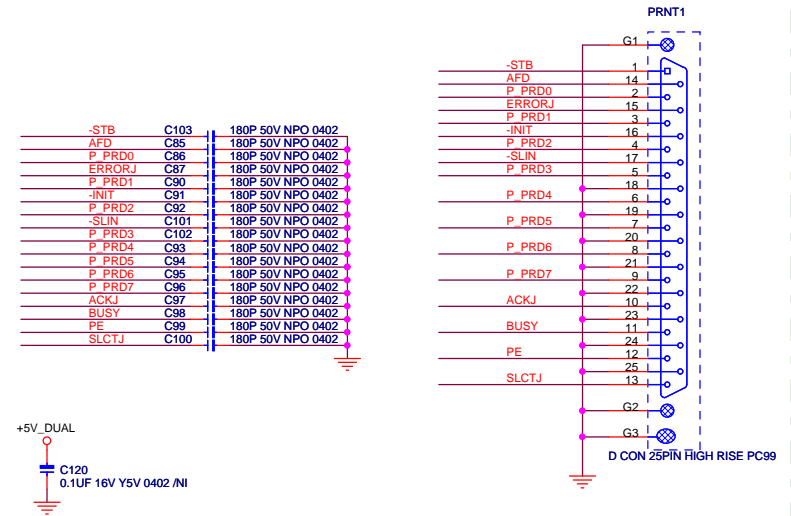
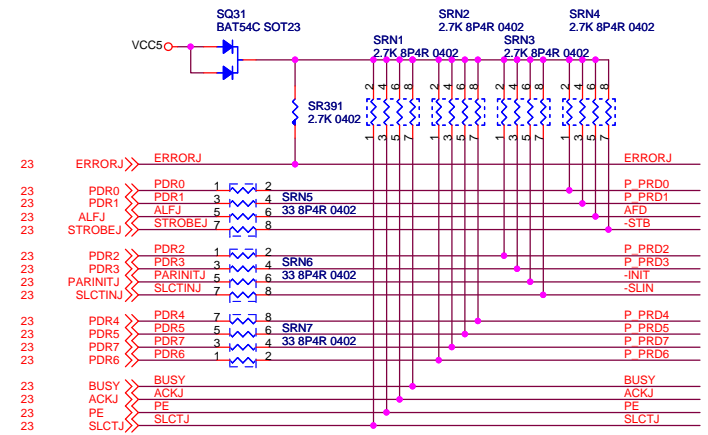
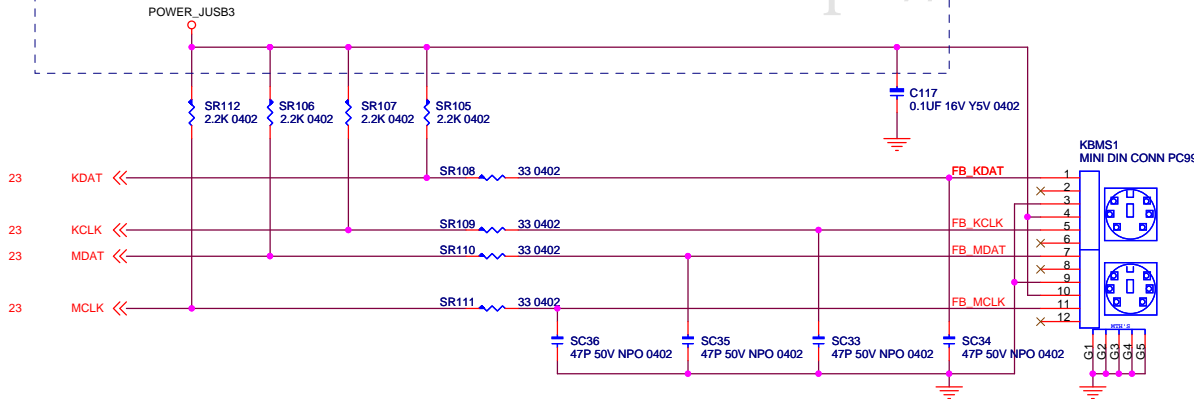


COM PORT

WAKE ON RING



VER0.6: COST DOWN (POWER_JUSB4/POWER_JUSB5 COLAY) (PAGE25/34)

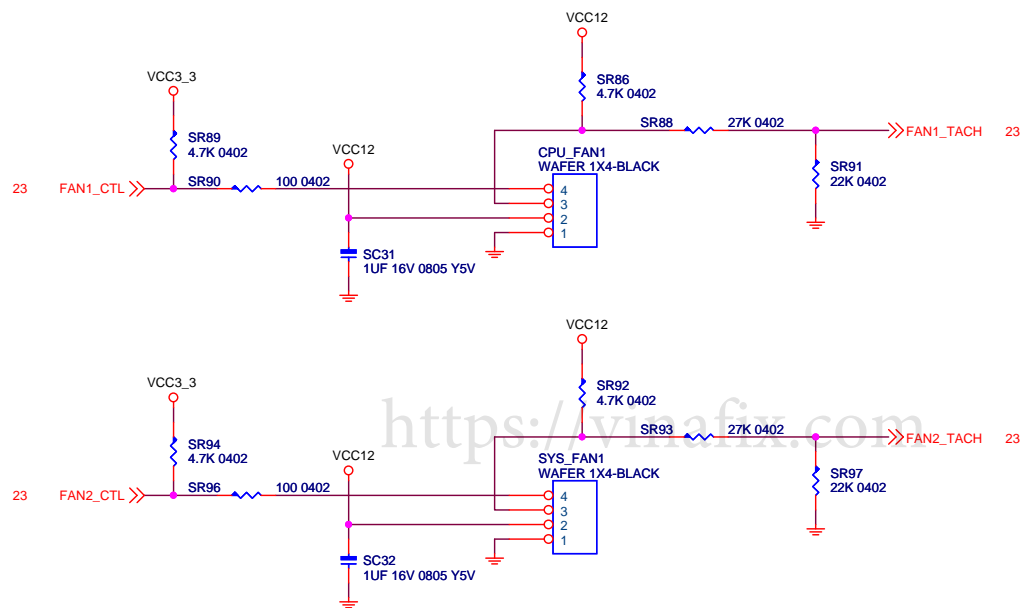


PARALLEL CONNECTOR

Vinafix.com

BIOSTAR'S PROPRIETARY INFORMATION

Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties.



◇BIOSTAR'S PROPRIETARY INFORMATION◇

◇Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties.◇



映泰股份有限公司
BIOSTAR GROUP

Title

FAN & PS2

Size
B

Document Number

IH11P-MHS

Rev
6.0

Date: Friday, January 15, 2016

Sheet 35 of 42

VCC12

FC3
470P 50V X7R 0402

VCC12-

FC1
470P 50V X7R 0402

VCC3_3

FC2
470P 50V X7R 0402

VCC5

FC4
470P 50V X7R 0402

VCC5

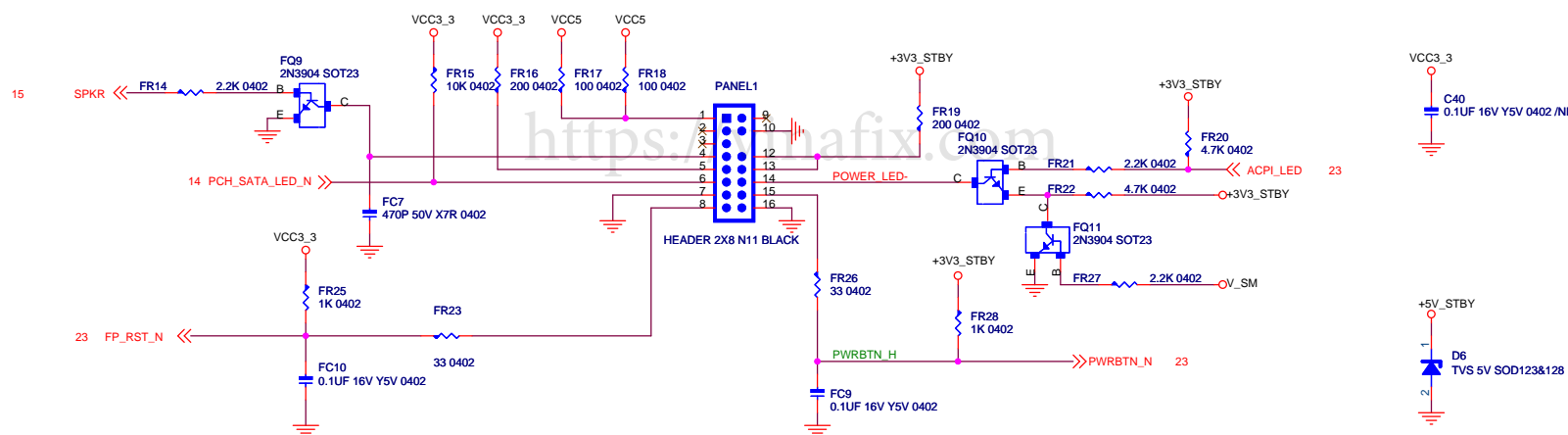
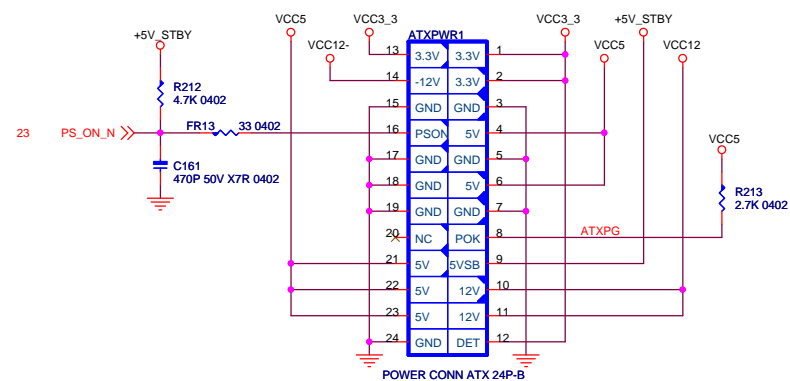
FC5
470P 50V X7R 0402

+5V_STBY

FC6
470P 50V X7R 0402

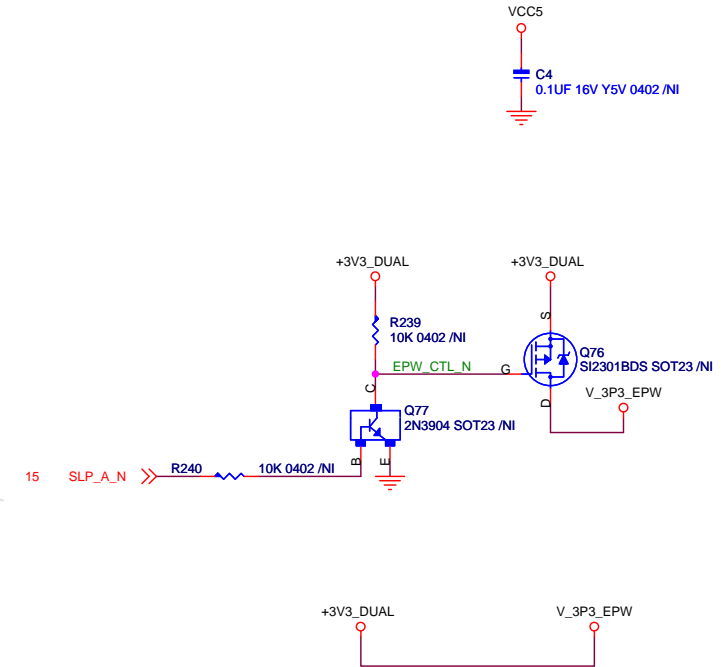
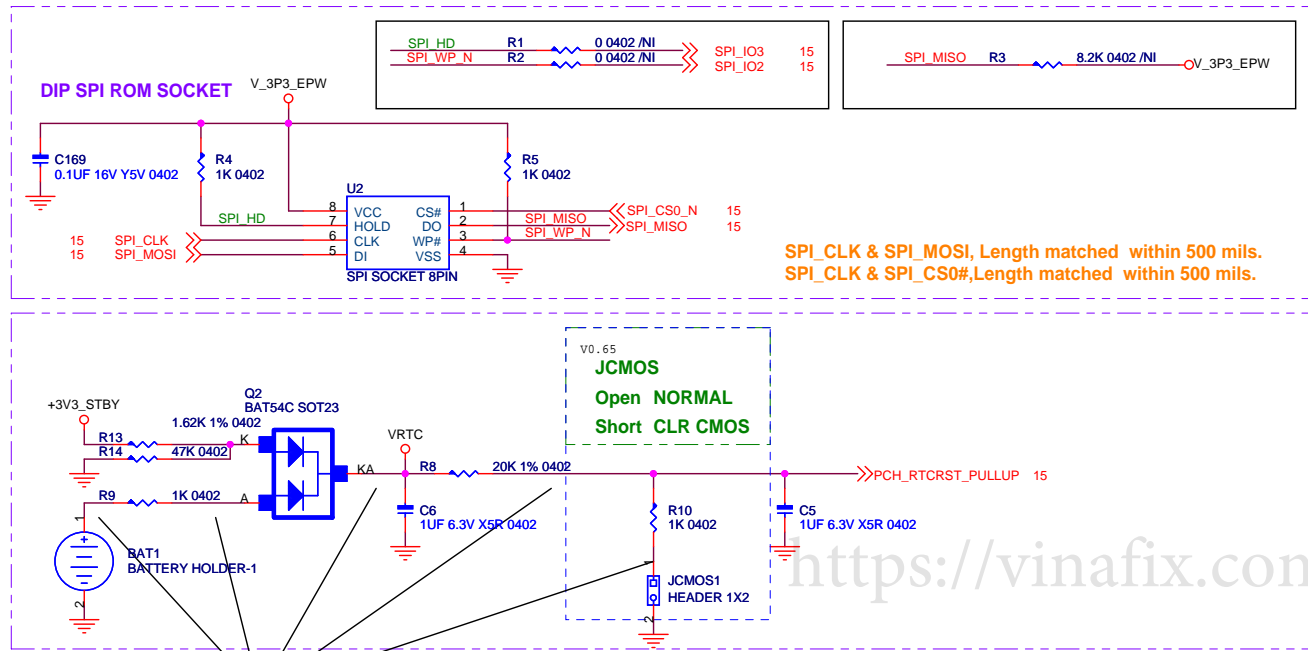
VCC5

CT13
560UF-S 6.3V 24M 6.3x9 BLK



◆Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties.◆



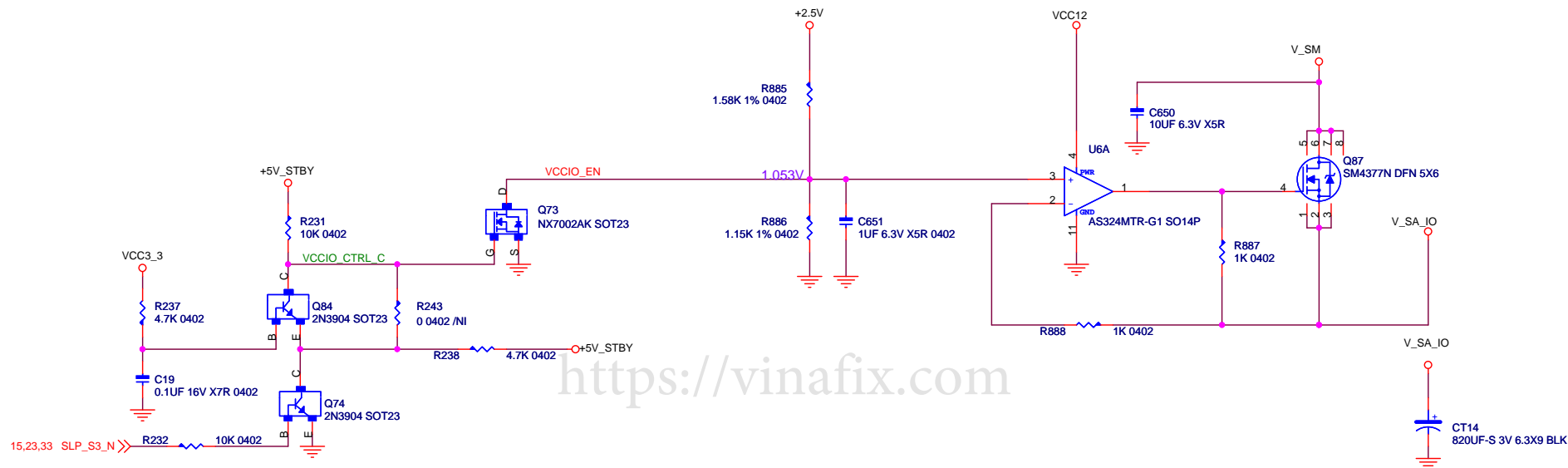


BIOSTAR'S PROPRIETARY INFORMATION

Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties.




Title			SPI ROM/RTC CRYSTAL/BAT	
Size	Document Number		IH11P-MHS	
B			Rev 6.0	
Date:	Friday, January 15, 2016		Sheet	37 of 42



<https://vinafix.com>

◇BIOSTAR'S PROPRIETARY INFORMATION◇

◇Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/orcriminal penalties.◇

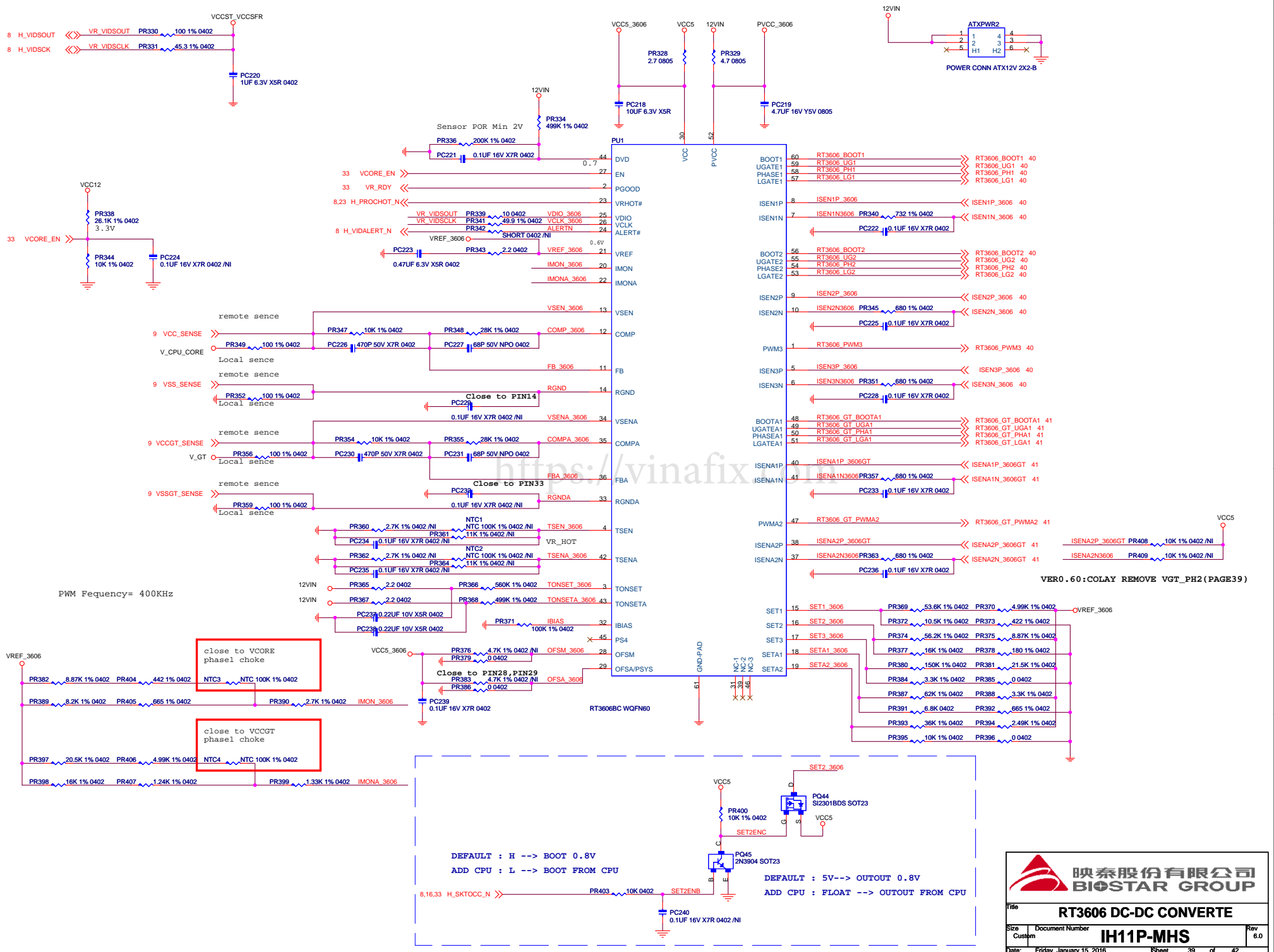


映泰股份有限公司
BIOSTAR GROUP

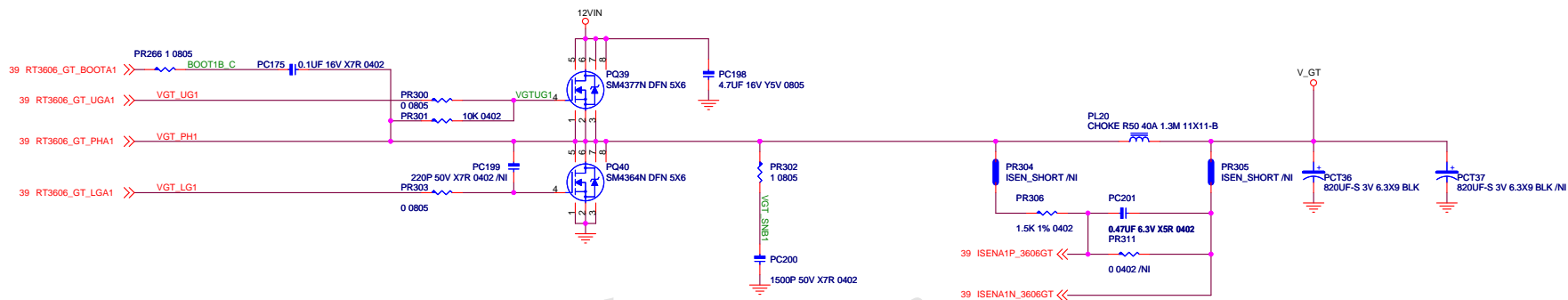
Title **VCCIO/VCCSA DC-DC**

Size B	Document Number IH11P-MHS	Rev 6.0
--------	----------------------------------	---------

Date: Friday, January 15, 2016 Sheet 38 of 42

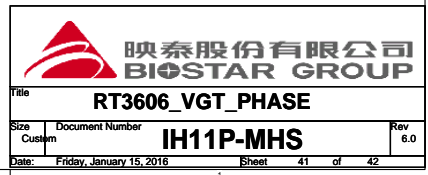
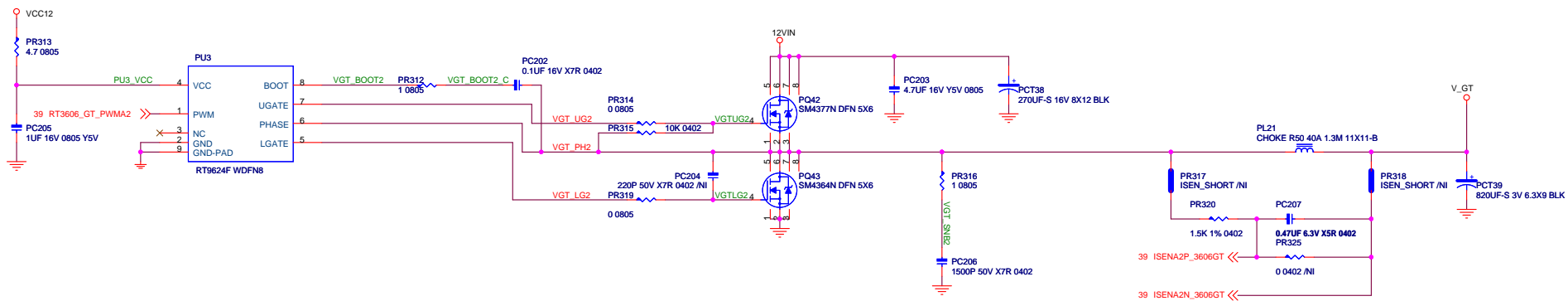


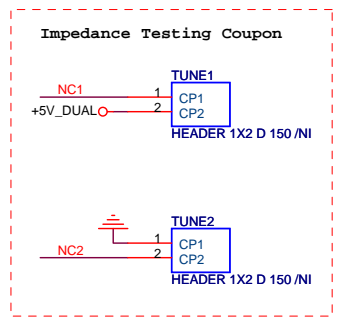
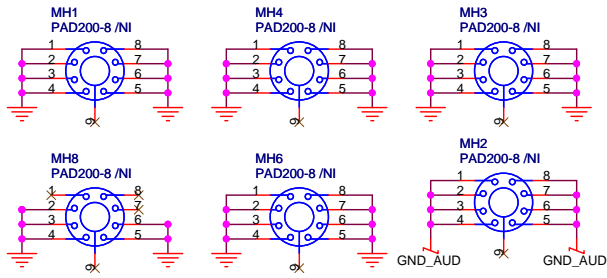
Skylake S-line 42 95W RT3606_VGT



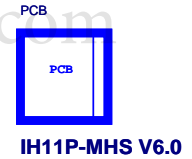
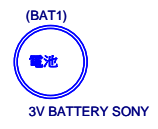
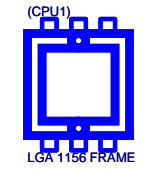
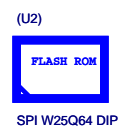
39 ISENA1N_3606GT


<https://vinafix.com>





<https://vinafix.com>





映泰股份有限公司
BIOSTAR GROUP

Title BOM		
Size B	Document Number IH11P-MHS	Rev 6.0
Date: Tuesday, January 19, 2016	Sheet 42	of 42